# SPECIFICATION
# FOR
# APPROVAL

(●) **Preliminary Specification**

( ) **Final Specification**

| Title | 30.0" HD OLED |
|---|---|

| BUYER | General |
|---|---|
| MODEL | |

| SUPPLIER | LG Display Co., Ltd. |
|---|---|
| *MODEL | LW300PXL |
| SUFFIX | HRT3 |

| APPROVED BY | SIGNATURE DATE |
|---|---|
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| / | |
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Please return 1 copy for your confirmation with your signature and comments.

| APPROVED BY | SIGNATURE DATE |
|---|---|
| Dong Kyu Yang / Team Leader | |
| **REVIEWED BY** | |
| Dong Il Kim / Project Leader | |
| **PREPARED BY** | |
| Sa Hwang Kim / Engineer | |

**OLED TV Development Dept.**
**LG Display Co., Ltd.**

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# RECORD OF REVISIONS

| Revision No. | Revision Date | Page | Description |
|---|---|---|---|
| 0.1 | Sep. 26. 2022 | - | Preliminary Specification (First Draft) |
| 0.2 | Oct.13 2022 | 7 | #17 PIN : TPC → NC<br>Update Note (Delete Note 5 about **#18** and **#19 Pin)** |
| | | 19 | Update T1 timing (15ms →16.5ms) |
| | | 20 | Modify Dclk 74.25 → 74.07MHz |
| | | 43 | Add ASIC Firmware |
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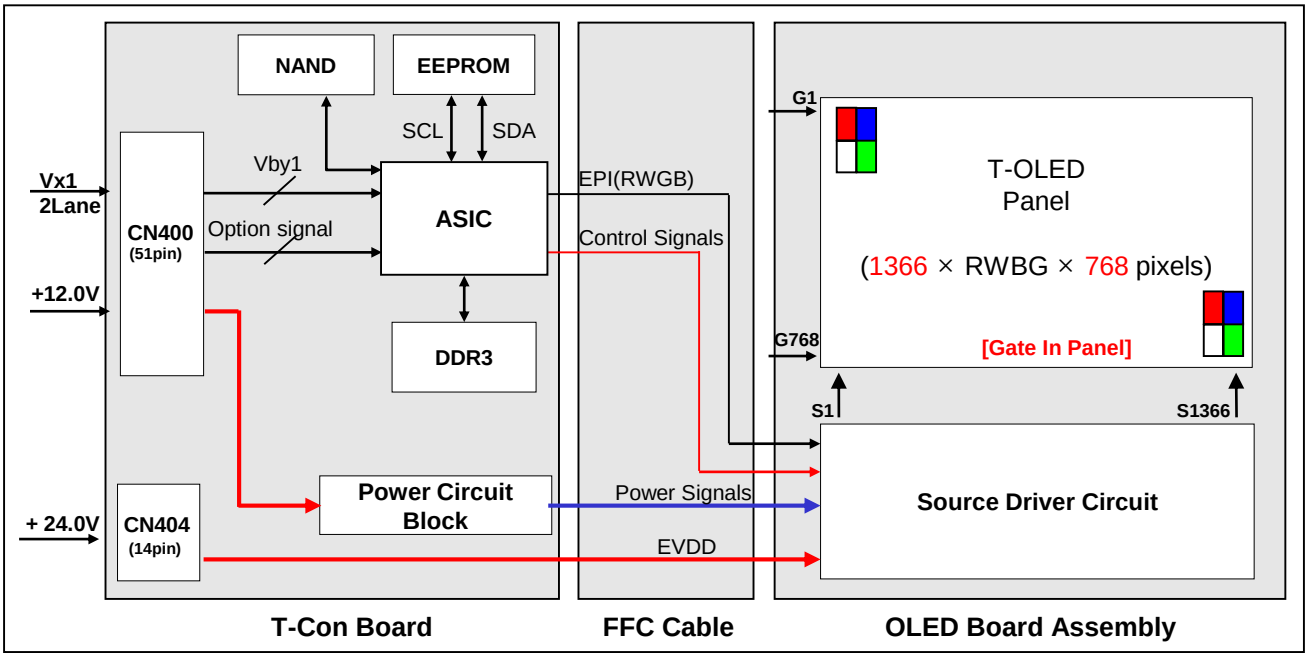
## 1. General Description

The LW300PLX is a Transparent Color Active Matrix Organic Light Emitting Diode Display (T-OLED).
The matrix employs Oxide Thin Film Transistor as the active element. It is a Top emission display type.
It has a 30 inch diagonally measured active display area with HD resolution (768 vertical by 1366 horizontal pixel array).
Each pixel is divided into Red, Green, Blue and White sub-pixels or dots which are arrayed in Quad.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07B(true) colors.
It has been designed to apply the 10-bit 2 Lane V by One interface.
It is intended to Public Display where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.




## General Features

| | |
|---|---|
| Active Screen Size | 30.00 inches(762.08mm) |
| Outline Dimension | 676.09(H) x 387.48 (V) mm (Typ.) |
| Pixel Pitch | 0.4863 mm x 0.4863 mm |
| Pixel Format | 1366 horiz. by 768 vert. Pixels, RWBG Quad arrangement |
| Color Depth | 10bit(R), 1.07Billon colors |
| Luminance, White | 350/135cd/m$^2$ (Center 1point ,Typ.) |
| Color Viewing Angle | R/L 120 (min.), U/D 120 (min.) (Δu'v' ≤ 0.026) |
| Power Consumption | Total W (Typ.) [Logic=10.56W, EVDD=8.9W @ IEC62087] (TBD) |
| Weight | 1.04kg (W/O C-PCB)(TBD) |
| Display Mode | Normally Transparent |
| Transparent Ratio | 43%(typ.) (TBD) |
| Reflectivity | 20% (typ.) (TBD) |
| Surface Treatment | Hard coating(2H) |

## 2. Absolute Maximum Ratings

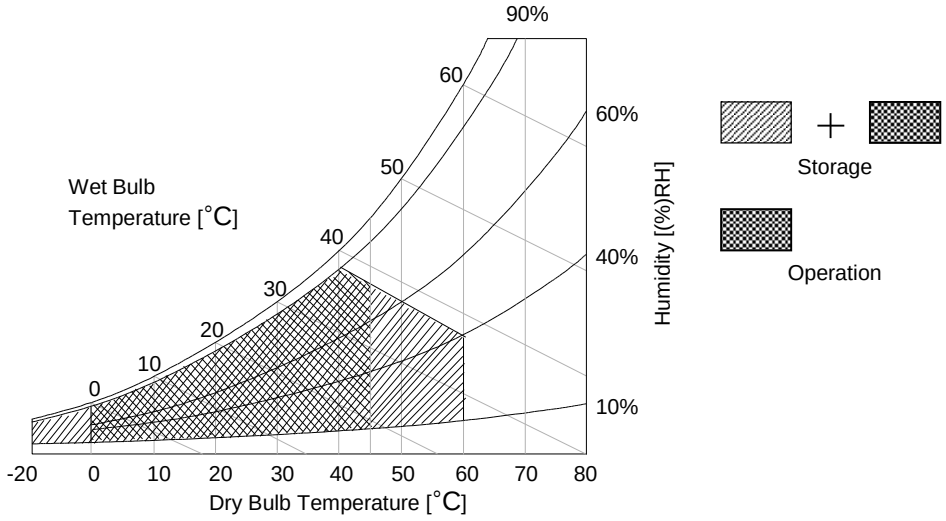
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the OLED module.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power Input Voltage | Logic | VDD | -0.3 | +14.0 | $V_{DC}$ | 1 |
| | OLED Panel | EVDD | -0.3 | +26(TBD) | $V_{DC}$ | |
| T-Con Option Selection Voltage | | $V_{LOGIC}$ | -0.3 | +3.7 | $V_{DC}$ | |
| Operating Temperature | | $T_{OP}$ | 0 | +45 | °C | 2 |
| Storage Temperature | | $T_{ST}$ | -20 | +60 | °C | |
| Operating Ambient Humidity | | $H_{OP}$ | 10 | 90 | %RH | 2 |
| Storage Humidity | | $H_{ST}$ | 10 | 90 | %RH | |

Notes

1. Ambient temperature condition (Ta = 25 ± 2 °C )
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.



## 3. Electrical Specifications

### 3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the circuit. The other is used for the EVDD.

| Parameter | Symbol | | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Power Input Voltage | VDD | | 10.8 | 12.0 | 13.2 | V | |
| | EVDD | | 21.9(TBD) | 23.0(TBD) | 24.2(TBD) | | |
| Power Input Current | $I_{VDD}$ | | - | 0.88(TBD) | 0.97(TBD) | A | 1-1/1-2 |
| | | | - | 1.21(TBD) | 1.33(TBD) | | 2 |
| | $I_{EVDD}$ | | - | 0.39(TBD) | 0.43(TBD) | | 1-1 |
| | | | - | 0.38(TBD) | 0.41(TBD) | | 1-2 |
| | | | - | 1.23(TBD) | 1.35(TBD) | | 3 |
| T-CON Option Voltage | $V_{IL}$ | | 0(TBD) | - | 0.8(TBD) | V | |
| | $V_{IH}$ | | 2.7(TBD) | - | 3.6(TBD) | V | |
| Power Consumption | $P_{VDD}$ | | - | 10.56(TBD) | 11.62(TBD) | Watt | 1-1/1-2 |
| | | | - | 14.52(TBD) | 15.97(TBD) | | 2 |
| | $P_{EVDD}$ | | - | 8.9(TBD) | 9.8(TBD) | | 1-1 |
| | | | - | 8.7(TBD) | 9.5(TBD) | | 1-2 |
| | | | - | 28.3(TBD) | 31.1(TBD) | | 3 |
| Rush current | $I_{RUSH}$ | $I_{RUSH\_VDD}$ | - | - | 7 (TBD) | A | 4 |
| | | $I_{RUSH\_EVDD}$ | - | - | 15 (TBD) | | |
| | | $T_{RUSH\_VDD}$ | - | - | 100 (TBD) | us | |
| | | $T_{RUSH\_EVDD}$ | - | - | 2 (TBD) | ms | |

Note

1-1. The specified current and power consumption are under the VDD=12.0V, EVDD=23.0V Ta=25 ± 2°C, $f_V$=120Hz, condition whereas standard moving picture(IEC62087) is displayed and $f_V$ is the frame frequency.

1-2 The specified current and power consumption are under the VDD=12.0V, EVDD=23.0V Ta=25 ± 2°C, $f_V$=120Hz condition whereas standard moving picture(CLASP) is displayed and $f_V$ is the frame frequency.

2. The current ($I_{VDD}$ ) is specified at the maximum current pattern (1by1 Horizontal Pattern) and under the VDD=12.0V, EVDD=23.0V Ta=25 ± 2°C condition.

3. The current ($I_{EVDD}$ ) is specified at the maximum current pattern (Secondary Color Pattern) and under the VDD=12.0V, EVDD=23.0V Ta=25 ± 2°C condition.

## 3-2. Interface Connections

This OLED module employs two kinds of interface connection, 51-pin connector is used for the module electronics and 14-pin connector is used for the EVDD.

### 3-2-1. OLED Module

- VDD Connector (CN400): FI-RE51S-HF(JAE)
- Mating Connector : FI-RE51HL(JAE) or compatible

**Table 3. MODULE CONNECTOR(CN400) PIN CONFIGURATION**

| No | Symbol | Description | No | Symbol | Description |
|---|---|---|---|---|---|
| 1 | VDD | Power Supply +12.0V | 27 | GND | Ground |
| 2 | VDD | Power Supply +12.0V | 28 | Rx0N | V-by-One HS Data Lane0 |
| 3 | VDD | Power Supply +12.0V | 29 | Rx0P | V-by-One HS Data Lane0 |
| 4 | VDD | Power Supply +12.0V | 30 | GND | Ground |
| 5 | NC (Reserved) | No Connection (Reserved) | 31 | Rx1N | V-by-One HS Data Lane1 |
| 6 | GND | Ground | 32 | Rx1P | V-by-One HS Data Lane1 |
| 7 | GND | Ground | 33 | GND | Ground |
| 8 | GND | Ground | 34 | NC (Reserved) | No Connection (Reserved) |
| 9 | GND | Ground | 35 | NC (Reserved) | No Connection (Reserved) |
| 10 | JB&Off-RS<br>Power_off done | JB&Off-RS&Power_off done (H),<br>Set ← Module (Note 3) | 36 | NC (Reserved) | No Connection (Reserved) |
| 11 | AC_DET | AC_DET (H= On), Set → Module | 37 | NC (Reserved) | No Connection (Reserved) |
| 12 | Error Detection | H' = Error , 'L' = Normal (note 4) | 38 | NC (Reserved) | No Connection (Reserved) |
| 13 | I2C_SDA1 | I2C for Customer | 39 | NC (Reserved) | No Connection (Reserved) |
| 14 | I2C_SCL1 | | 40 | NC (Reserved) | No Connection (Reserved) |
| 15 | NC (Reserved) | No Connection (Reserved) | 41 | NC (Reserved) | No Connection (Reserved) |
| 16 | NC (Reserved) | No Connection (Reserved) | 42 | NC (Reserved) | No Connection (Reserved) |
| 17 | NC (Reserved) | No Connection (Reserved) | 43 | NC (Reserved) | No Connection (Reserved) |
| 18 | I2C_SDA | I2C for Customer | 44 | NC (Reserved) | No Connection (Reserved) |
| 19 | I2C_SCL | | 45 | NC (Reserved) | No Connection (Reserved) |
| 20 | EVDD_DET | EVDD reset, Set ← Module | 46 | NC (Reserved) | No Connection (Reserved) |
| 21 | NC (Reserved) | No Connection (Reserved) | 47 | NC (Reserved) | No Connection (Reserved) |
| 22 | GND | AGP2 (note 6) | 48 | NC (Reserved) | No Connection (Reserved) |
| 23 | GND | AGP1 (note 6) | 49 | QSMEN | QSMEN (Set→Module) |
| 24 | GND | Ground | 50 | ON_RF | On_RF_Done (Set ← Module) |
| 25 | HTPDN | Hot plug detect | 51 | NC (Reserved) | No Connection (Reserved) |
| 26 | LOCKN | Lock detect | - | - | - |

Notes

1. All GND(ground) pins should be connected together.
2. All Input levels of V-by-One signals are based on the V-by-One HS Standard.
3. Specific pin No. **#10** is used for compensation when Power turn off.
4. Specific pin No. **#12** is used for "Power Error detection" of the OLED module.
5. Specific pins No. **#22** and **#23** are used for "No signal detection" of system signal interface.
   It should be GND for NSB (No Signal Black) while the system interface signal is not.
   If this pin is "H" or "NC", OLED module displays AGP (Auto Generation Pattern).

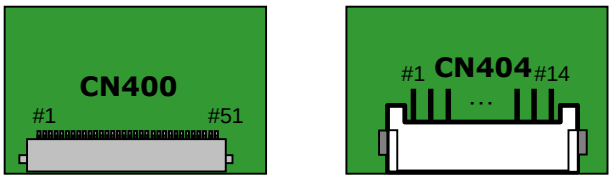
### 3-2-2. OLED Module (EVDD)

- EVDD Connector (CN404) : 20022WR-H14B2 (manufactured by Yeon Ho)
- Mating Connector : 2022HS-14B2(BK) (manufactured by Yeon Ho)

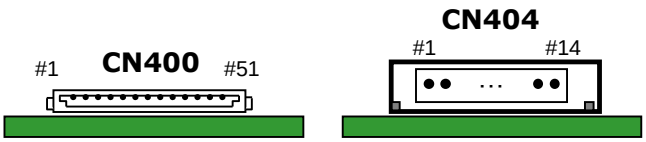
**Table 4. EVDD CONNECTOR(CN404) PIN CONFIGURATION**

| No | Symbol | Description |
|---|---|---|
| 1 | EVSS | OLED Panel Ground |
| 2 | EVSS | OLED Panel Ground |
| 3 | EVSS | OLED Panel Ground |
| 4 | EVSS | OLED Panel Ground |
| 5 | EVSS | OLED Panel Ground |
| 6 | EVSS | OLED Panel Ground |
| 7 | NC | Don't care |
| 8 | EVDD | OLED Panel Power Supply +23V |
| 9 | EVDD | OLED Panel Power Supply +23V |
| 10 | EVDD | OLED Panel Power Supply +23V |
| 11 | EVDD | OLED Panel Power Supply +23V |
| 12 | EVDD | OLED Panel Power Supply +23V |
| 13 | EVDD | OLED Panel Power Supply +23V |
| 14 | EVDD | OLED Panel Power Supply +23V |

◆ **Rear view of OLED Module**




< Top view of PCB >




< Side view of PCB >

## 3-3. Signal Timing Specifications

Table 6-1 shows the signal timing required at the input of the **Vx1** transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

**Table 6-1. TIMING TABLE (DE Only Mode)**

| ITEM | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Horizontal** | Display Period | tHV | 683 | 683 | 683 | tCLK | 1366/2 |
| | Blank | tHB | 65 | 67 | 68 | tCLK | 1 |
| | | | 0.875 | 0.905 | 0.921 | us | 3 |
| | Total | tHP | 748 | 750 | 751 | tCLK | |
| **Vertical** | Display Period | tVV | 768 | 768 | 768 | Lines | |
| | Blank | tVB | 54 | 55 | 60 | Lines | 1 |
| | | | (200) | (220) | (271) | | |
| | | | 542.9 | 556.9 | 614.1 | us | 3 |
| | | | (2010.8) | (2227.6) | (2773.7) | | |
| | Total | tVP | 822 (968) | 823 (988) | 828 (1039) | Lines | |

| ITEM | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Frequency** | DCLK | fCLK | 73.82 | 74.07 | 74.32 | MHz | 148.14/2 |
| | Horizontal | fH | 97.704 | 98.760 | 99.462 | KHz | 1 |
| | Vertical | fV | 118 (95.05) | 120 (99.96) | 121 (102) | Hz | 2 NTSC (PAL) |

Notes:

1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency.
3. If you change the DCLK, must satisfy the minimum horizontal & vertical blank time.

※ This OLED module supports Spread Spectrum Clocking tolerance with up to 40kHz / **±0.5%**

※ Timing should be set based on clock frequency.

**Table 6-2. Timing Table(Only Gaming mode : VRR Mode)**

| ITEM | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Horizontal** | Display Period | $t_{HV}$ | 683 | 683 | 683 | tCLK | 1366/2 |
| | Blank | $t_{HB}$ | 67 | 67 | 67 | tCLK | |
| | Total | $t_{HP}$ | 750 | 750 | 750 | tCLK | |
| **Vertical** | Display Period | $t_{VV}$ | 768 | 768 | 768 | Lines | |
| | Blank | $t_{VB}$ | 55 | 55 | 1701 | Lines | |
| | Total | $t_{VP}$ | 823 | 823 | 2469 | Lines | |

| ITEM | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Frequency** | DCLK | $f_{CLK}$ | 74.07 | 74.07 | 74.07 | MHz | 148.14/2 |
| | Horizontal | $f_{H}$ | 98.760 | 98.760 | 98.760 | KHz | |
| | Vertical | $f_{V}$ | 40 | 120 | 120 | Hz | |

Note:
1. Only applicable to Gaming mode with VRR operation
2. The device could not work properly in case it is operated by VRR mode.
   1) This OLED module supports adaptive sync timing only under moving picture in room temperature(25±5℃)
   2) It would not work usually under still image & reliability test.
   3) Under those condition, the phenomenon such as image sticking, flickering, flashing and dither noise in low gray could be found on the screen.

## 3-4. V by One input Signal Characteristics

### 3-4-1. V by One Input Signal Timing Diagram

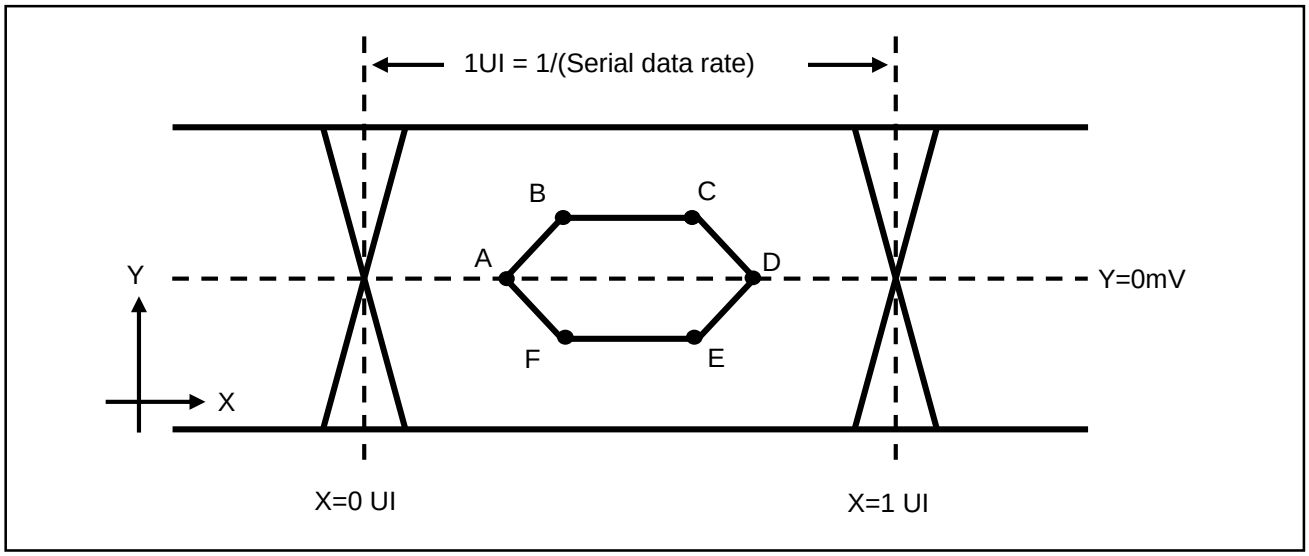
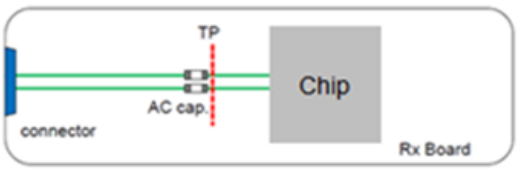



**Table 7. Eye Mask Specification**

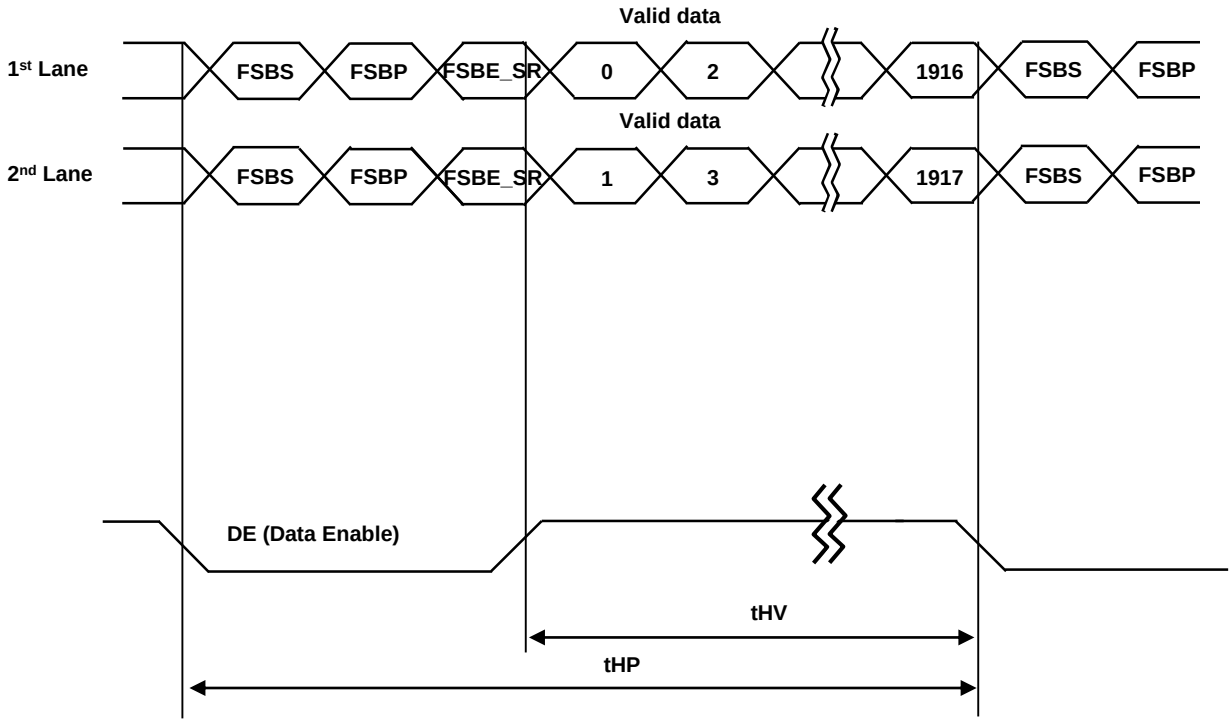
| | X [mV] | Note | Y [UI] | Note |
|---|---|---|---|---|
| A | 0.25 (max) | 2 | 0 | - |
| B | 0.30 (max) | 2 | 50 | 3 |
| C | 0.70 (min) | 3 | 50 | 3 |
| D | 0.75 (min) | 3 | 0 | - |
| E | 0.70 (min) | 3 | \|-50\| | 3 |
| F | 0.30 (max) | 2 | \|-50\| | 3 |

Notes

1.1 All Input levels of V by One signals are based on the V by One HS Standard.
1.2 When using the Tx's Pre-Emphasis function to be set to a minimum value that meets the EYE Mask Spec
2. This is allowable maximum value.
3. This is allowable minimum value
4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
   - PLL Type : 2nd Order
   - PLL bandwidth : 10MHz
   - Damping Factor : 2
5. EYE mask measuring point

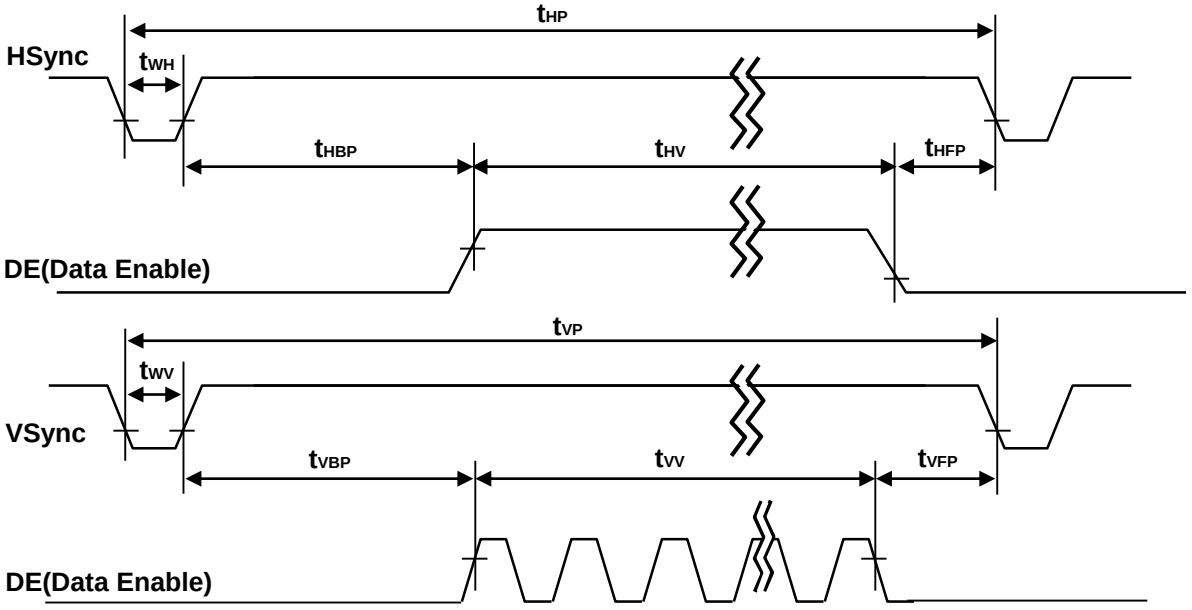


### 3-4-2. V by One Input Signal Timing Diagram



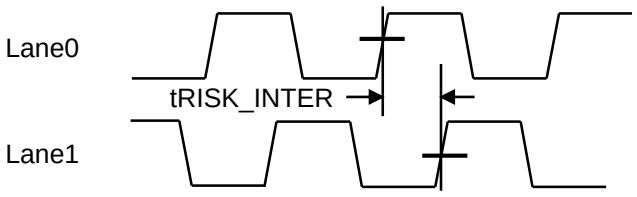

## * Reference: Sync. Relation

* tHB = tHFP + tWH +tHBP
* $t_{VB}$ = $t_{VFP}$ + $t_{WV}$ +$t_{VBP}$

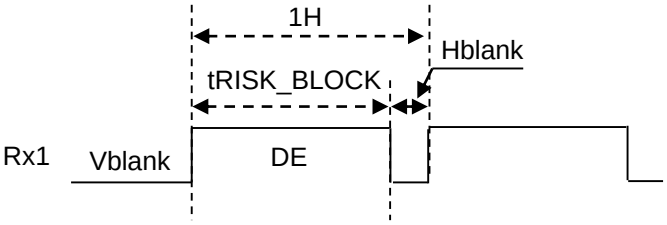


### 3-4-3. V by One Input Signal Characteristics

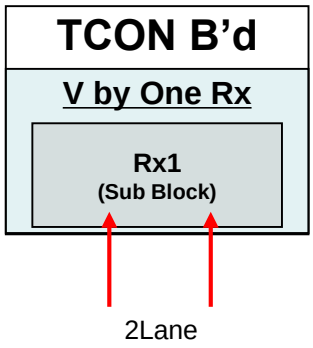
#### 1) AC Specification




<Inter-pair skew between two lanes>




<Inter-pair skew between two sub-blocks>




<V by One Brief Diagram >

| Description | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Allowable inter-pair skew between lanes | tRISK_INTER | - | 5 | UI | 1, 3 |
| Allowable inter-pair skew between sub-blocks | tRISK_BLOCK | - | 1 | DE | 1, 4 |

Notes: 1.1UI = 1/serial data rate
2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.
5. APL packet of Vx1 Input
   5-1) APL data transmission should be completed between after 5H from frame last DE falling and 10H before next frame DE rising.
   5-2) APL data transmission should be inputted only one time during V blank period.

## 3-5. Color Data Reference

The brightness of each primary color (red,green,blue) is based on the 10bit gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data input.

**Table 8. COLOR DATA REFERENCE**

| Packer input & Unpacker output | | 30bpp RGB (10bit) |
|---|---|---|
| Byte0 | D[0] | R[2] |
| | D[1] | R[3] |
| | D[2] | R[4] |
| | D[3] | R[5] |
| | D[4] | R[6] |
| | D[5] | R[7] |
| | D[6] | R[8] |
| | D[7] | R[9] |
| Byte1 | D[8] | G[2] |
| | D[9] | G[3] |
| | D[10] | G[4] |
| | D[11] | G[5] |
| | D[12] | G[6] |
| | D[13] | G[7] |
| | D[14] | G[8] |
| | D[15] | G[9] |
| Byte2 | D[16] | B[2] |
| | D[17] | B[3] |
| | D[18] | B[4] |
| | D[19] | B[5] |
| | D[20] | B[6] |
| | D[21] | B[7] |
| | D[22] | B[8] |
| | D[23] | B[9] |
| Byte3 | D[24] | Don't care |
| | D[25] | Don't care |
| | D[26] | B[0] |
| | D[27] | B[1] |
| | D[28] | G[0] |
| | D[29] | G[1] |
| | D[30] | R[0] |
| | D[31] | R[1] |

Notes 1. 30bpp RGB (10bit) is 4 byte mode

## 3-6. Power Sequence

### 3-6-1. OLED Driving circuit

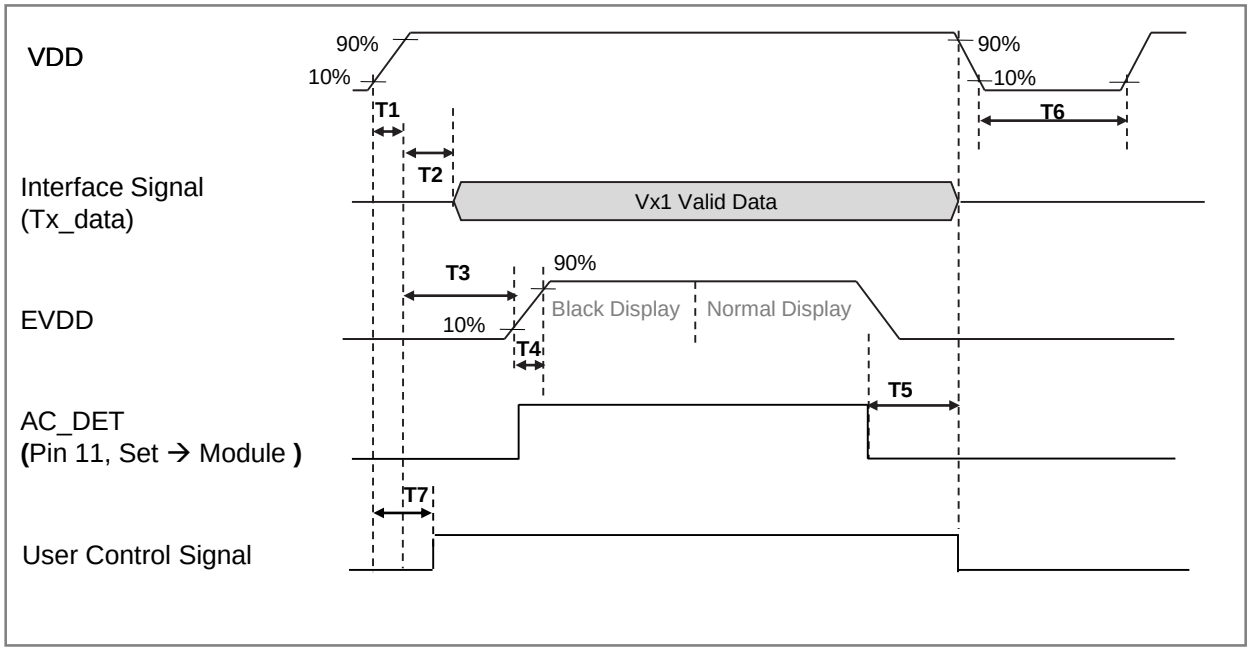



**Table 9. POWER SEQUENCE**

| Parameterz | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 1(TBD) | - | 20(TBD) | ms | 1 |
| T2 | 58(TBD) | - | - | ms | |
| T3 | 0.6(TBD) | - | - | sec | 2 |
| T4 | 5(TBD) | - | 50(TBD) | ms | |
| T5 | 30(TBD) | - | - | ms | |
| T6 | 1.5(TBD) | - | - | sec | 3 |
| T7 | 0(TBD) | - | T1+T2(TBD) | ms | 4 |

Notes

1. The T3 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem. T3 should be larger than T2.
2. T6 should be measured after the module has been fully discharge between power off and on period.
3. If the on time of signals (Interface signal and user control signals) precedes the on time of Power(VDD) it will be happened abnormal display. When T7 is NC status, T7 doesn't need to be measured
4. I2C is able to be accessed from 540ms after VDD 90% rising

※ Black pattern is displayed during black display period before normal display. (ON RF Time 2.7S(TBD))

※ When the power for logic (VDD_12V) turns off, EVDD should be less than 8.0V. But, it does not matter if there is no garbage image.

### 3-6-2. OFF RS Compensation Operation

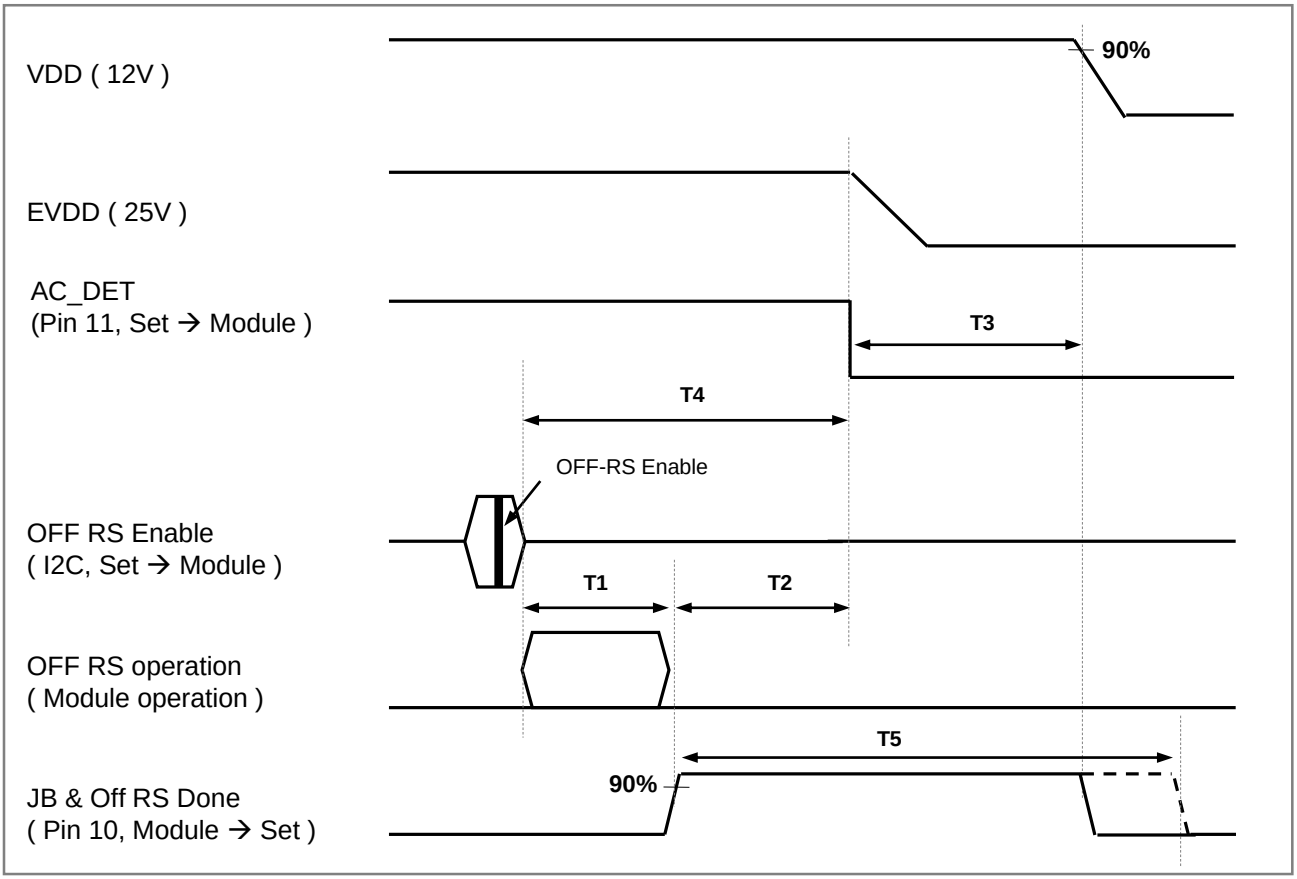



**Table 10. POWER SEQUENCE**

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 100(TBD) | - | 170(TBD) | sec | 1 |
| T2 | 0(TBD) | - | 10(TBD) | sec | |
| T3 | 30(TBD) | - | - | ms | |
| T4 | 180(TBD) | - | - | sec | 2 |
| T5 | 0.5(TBD) | 7(TBD) | 10(TBD) | sec | |

Note : 1. It is the actual RS sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)

2. TV system is recommended to be turned off **immediately** after T4 **min.** although Off-RS Done signal is not transferred.

※ When there is power on action before completing OFF RS operation, don't change OFF RS enable signal (1→0). Just do power off and power on.

※ Off RS Enable is only available during Normal Display period

※ In order to prevent mura defects, it is recommended that customer do Off-RS in their lines.

### 3-6-3. JB compensation operation

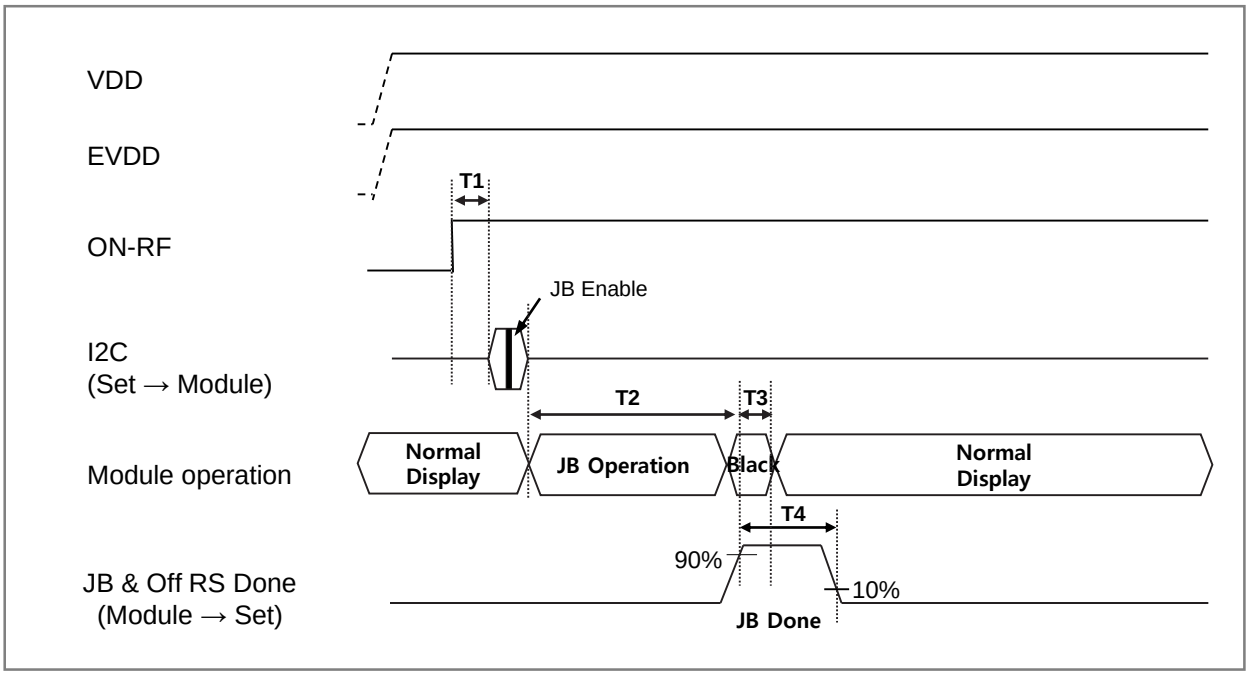
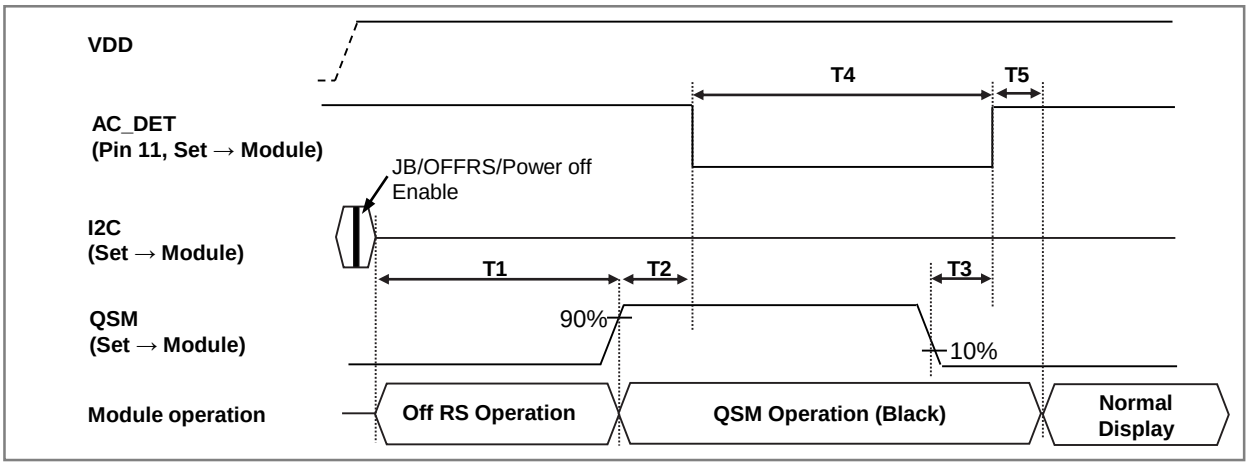



**Table 11. JB Power Sequence**

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 200(TBD) | - | - | ms | |
| T2 | 2(TBD) | - | 15(TBD) | sec | |
| T3 | 415.6(TBD) | - | 508.0(TBD) | ms | Black PTN |
| T4 | 0.5(TBD) | 7 | 10(TBD) | sec | |

Note : ※ JB Compensation must be operated in the temperature range of JB operation, 10 to 40℃
※ At VRR mode, T3 can change by adaptive sync timing(T3 need 19 frame ) (VRR only)
※ T2 is the actual JB sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)

### 3-6-4. QSM Operation




### Table 12. QSM Sequence

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 3(TBD) | - | - | sec | JB/OFFRS |
| | 1(TBD) | - | - | sec | POWER OFF |
| T2 | 75 (TBD) | - | - | ms | |
| T3 | 10(TBD) | - | - | ms | |
| T4 | 1(TBD) | - | - | sec | |
| T5 | 200(TBD) | - | 500(TBD) | ms | |

**3-6-5.** Power off sequence

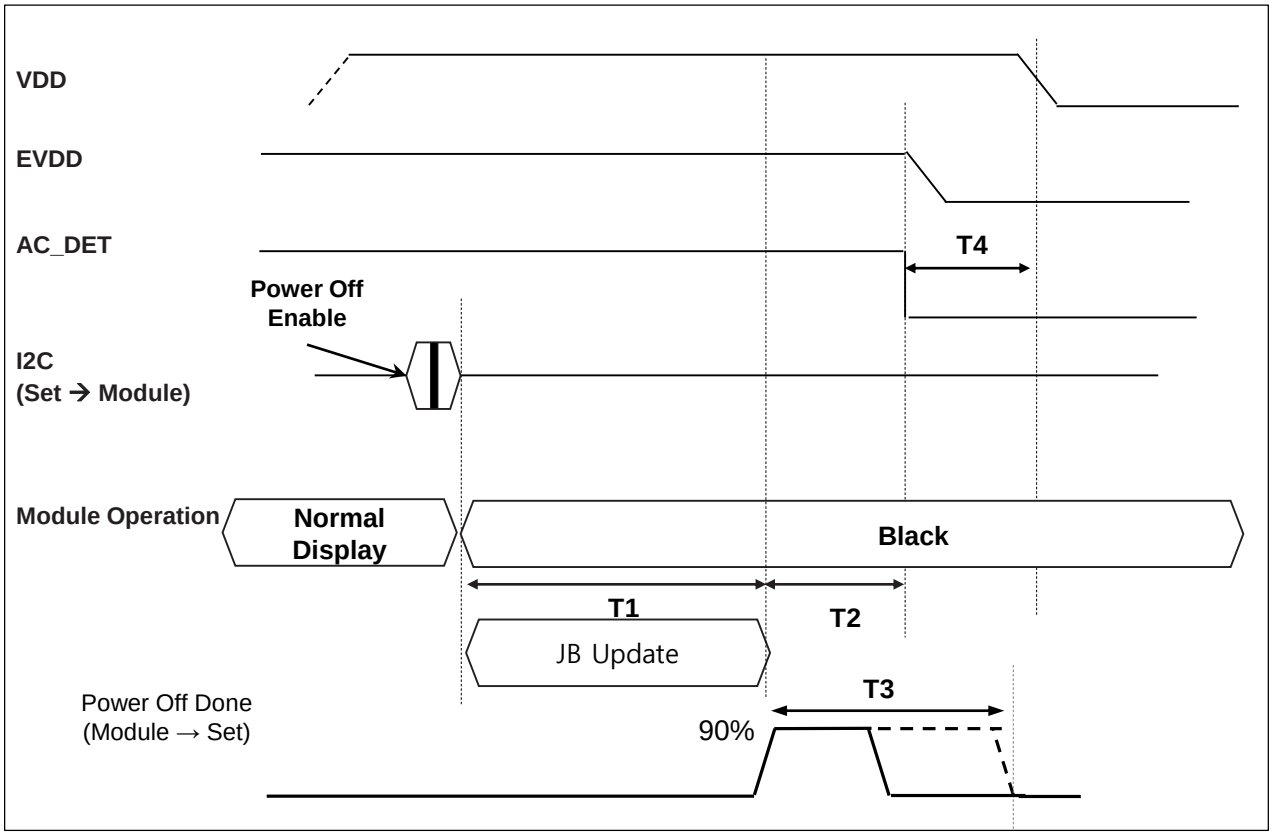



**Table 13. POWER SEQUENCE**

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | - | - | 16.5(TBD) | sec | |
| T2 | 30(TBD) | - | - | ms | |
| T3 | 5(TBD) | 7(TBD) | 10(TBD) | sec | |
| T4 | 30(TBD) | - | - | ms | |

## 4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the OLED surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

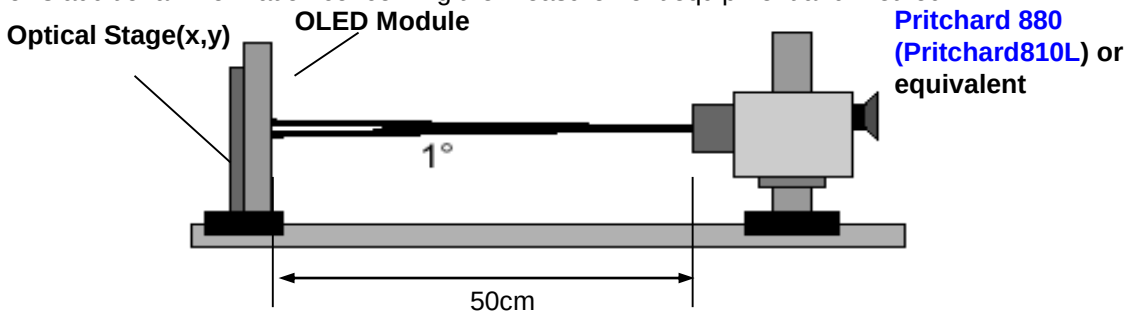



**FIG. 1 Optical Characteristic Measurement Equipment and Method**

**Table 14. OPTICAL CHARACTERISTICS** Ta= 25±2°C, VDD=12.0V, EVDD=23V, fv=120Hz, Dclk=74.07MHz

| Parameter | | Symbol | | | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| Contrast Ratio | | CR @ Pritchard 880 | | | 108,000(TBD) | 135,000(TBD | - | | 1 |
| | | CR @ Pritchard 810L (25% APL) | | | 840,000 (TBD) | 1,050,000 (TBD) | | | |
| Surface Luminance, white | | $L_{WH}$ | 2D | Normal | 108(TBD) | 135(TBD) | | cd/m² | 2 |
| | | | | Peak | 280(TBD) | 350(TBD) | | | |
| Luminance Uniformity | | $\delta_{WHITE}$ | 9P | | 70(TBD) | 80(TBD) | - | % | 3 |
| Response Time | Gray-to-Gray | G to G | | | - | 0.1(TBD) | 3 | ms | 4 |
| | MPRT | MPRT | | | - | 8(TBD) | 12 | ms | 5 |
| Color Coordinates [CIE1931] | RED | Rx | | | Typ -0.02 | 0.669(TBD) | Typ +0.02 | | |
| | | Ry | | | | 0.327(TBD) | | | |
| | GREEN | Gx | | | | 0.307(TBD) | | | |
| | | Gy | | | | 0.651(TBD) | | | |
| | BLUE | Bx | | | | 0.150(TBD) | | | |
| | | By | | | | 0.059(TBD) | | | |
| | WHITE | Wx | | | | 0.285(TBD) | | | |
| | | Wy | | | | 0.294(TBD) | | | |
| Color Temperature | | | | | | 9,300(TBD) | | K | |
| Color Gamut (DCI) | | | | | | 90(TBD) | | % | |
| Color Viewing Angle | | | | | | | | | |
| (Δu'v' ≤ 0,026) | x axis, right(ϕ=0°) | θr | | | 60 | - | - | degree | 6 |
| | x axis, left (ϕ=180°) | θl | | | 60 | - | - | | |
| | y axis, up (ϕ=90°) | θu | | | 60 | - | - | | |
| | y axis, down (ϕ=270°) | θd | | | 60 | - | - | | |
| Life Time (B10) | | Hrs | | | - | 30,000 | - | | 7 |
| Gray Scale | | | | | | 2.2 | | | 8 |

Notes : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Normal full white luminance is determined with 100% APL after 30 minutes 'ON' with WRGB rolling pattern in a dark environment at 25±2°C . It is the luminance value at center 1-point across the OLED surface 50cm from the surface with all pixels displaying white. Peak luminance is determined with 25% APL after 60 seconds at least 'ON' with 25% white window box.
   ※ Normal : APL 100% (Full white) / Peak : APL 25%
3. The variation in surface luminance , δ WHITE is defined as :
   δ WHITE(9P) = Minimum($L_{on1}$,.... $L_{on9}$) / Maximum($L_{on1}$..... $L_{on9}$)
   Where $L_{on1}$ to $L_{on9}$ are the luminance with all pixels displaying white at 9 locations .
   For more information, see the FIG. 2.
4. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, $Tr_R$) and from G(M) to G(N) (Decay Time, $Tr_D$). For additional information see the FIG. 3. (N<M)
   ※ G to G Spec stands for average value of all measured points.
   ※ Test equipment : PR-810, Test Distance : Display Height * 0.35
   Measuring Field : 1°, Test Pattern : APL10% Window Box
5. MPRT is defined as the 10% to 90% blur-edge width Bij(pixels) and scroll speed U(pixels/frame)at the moving picture. For more information, see FIG 4
6. Viewing Angle Color Shift (VACS) is defined as follows after measuring color coordinates at each angle.; VACS=sqrt(du3+dv3) (@ CIE (u', v') color space) For more information, see the FIG. 5.
7. Test Condition : IEC62087 standard video with OFF-RS every 4 hours at room temperature 25℃
   (If the cumulative time of usage is over 4 hours, OFF-RS compensation should be performed.)
8. Gray scale specification. Gamma Value is approximately 2.2. For more information, see the Table 15.

**Table 15. GRAY SCALE SPECIFICATION**

| Gray Level | Luminance [%] (Typ) |
|---|---|
| L0 | 0.001 |
| L63 | 0.20 |
| L127 | 0.97 |
| L191 | 2.42 |
| L255 | 4.61 |
| L319 | 7.59 |
| L383 | 11.4 |
| L447 | 16.0 |
| L511 | 21.6 |
| L575 | 28.0 |
| L639 | 35.4 |
| L703 | 43.7 |
| L767 | 53.0 |
| L831 | 63.2 |
| L895 | 74.5 |
| L959 | 86.7 |
| L1023 | 100 |

Measuring point for surface luminance & measuring point for luminance variation.

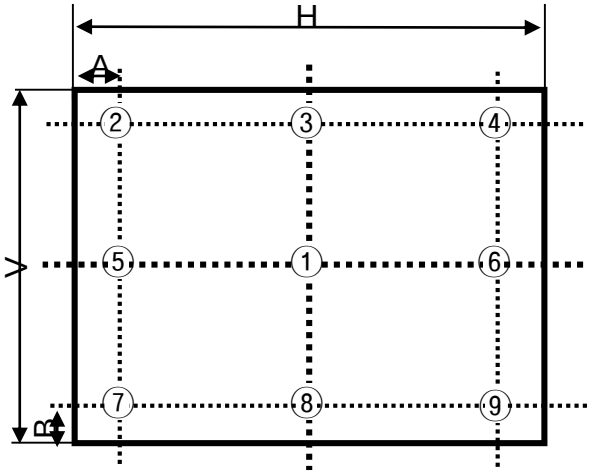



**FIG. 2-1 9 Points for Luminance Measure with 100% APL**

A: H/9 B: V/9 @ H,V: Active Area

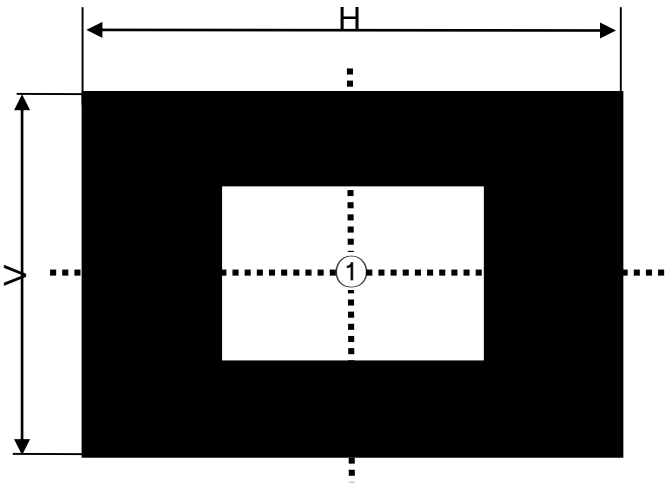
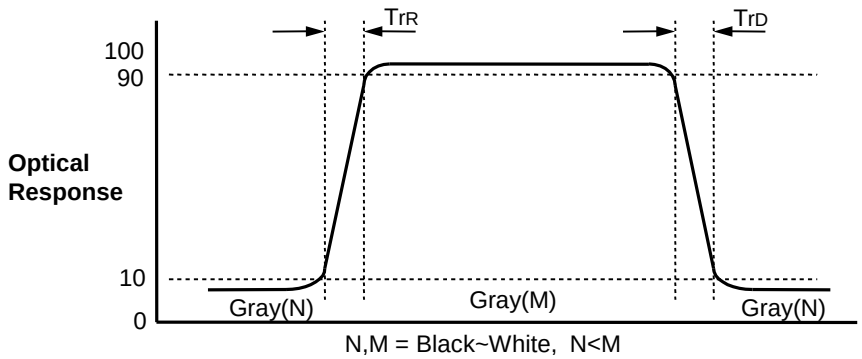



**FIG. 2-2. 1 Points for peak luminance measure with 25% APL**

@ H,V: Active Area

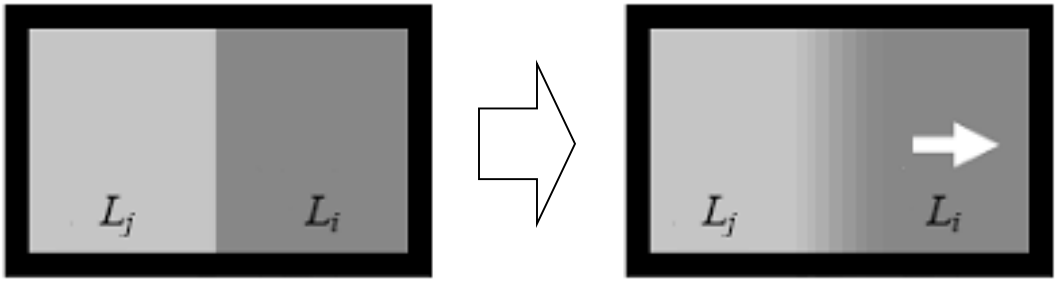
Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".



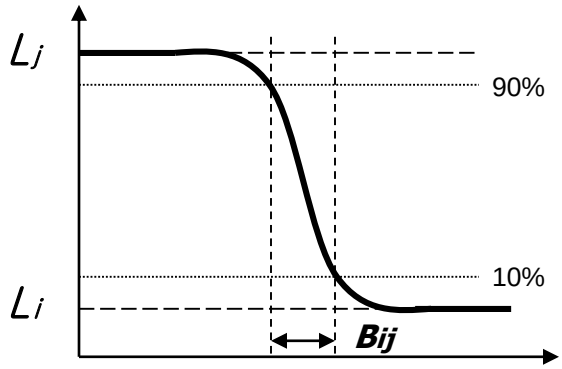

N,M = Black~White, N<M

**FIG. 3 Response Time**

MPRT is defined as the 10% to 90% blur-edge with Bij(pixels) and scroll speed U(pixels/frame)at the moving picture.




$$M = \frac{1}{U} Bij \ (i \neq j)$$




Example) Bij = 12pixels, U = 10pixels / 120Hz
M = 12pixels / (10pixels / 120Hz)
= 12pixels / {10pixels / (1/120)s}
= 12 / 1,200 s
= 10 ms

**FIG. 4 MPRT**

Dimension of viewing angle range

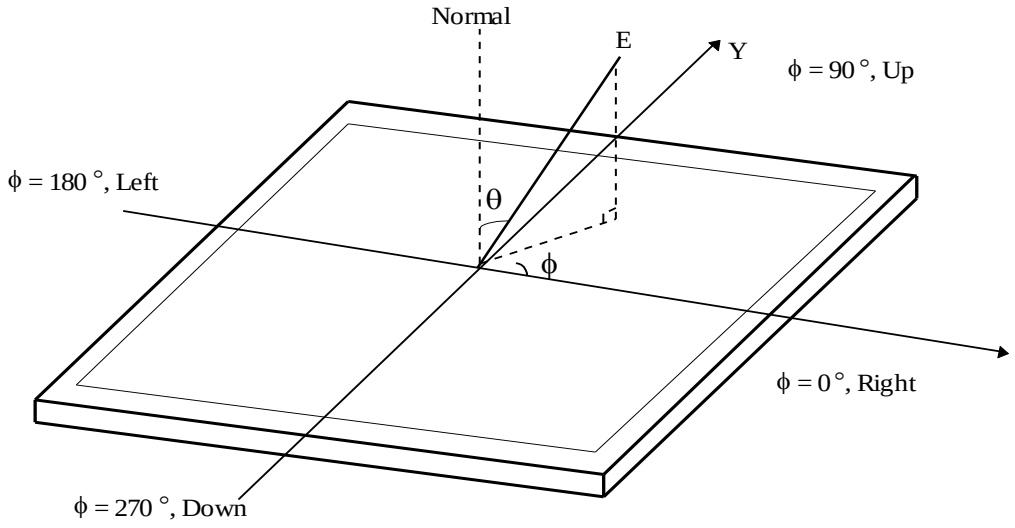



**FIG. 5 Viewing Angle**

## 5. Mechanical Characteristics

Table 16 provides general mechanical characteristics.

**Table 16. Mechanical Characteristics**

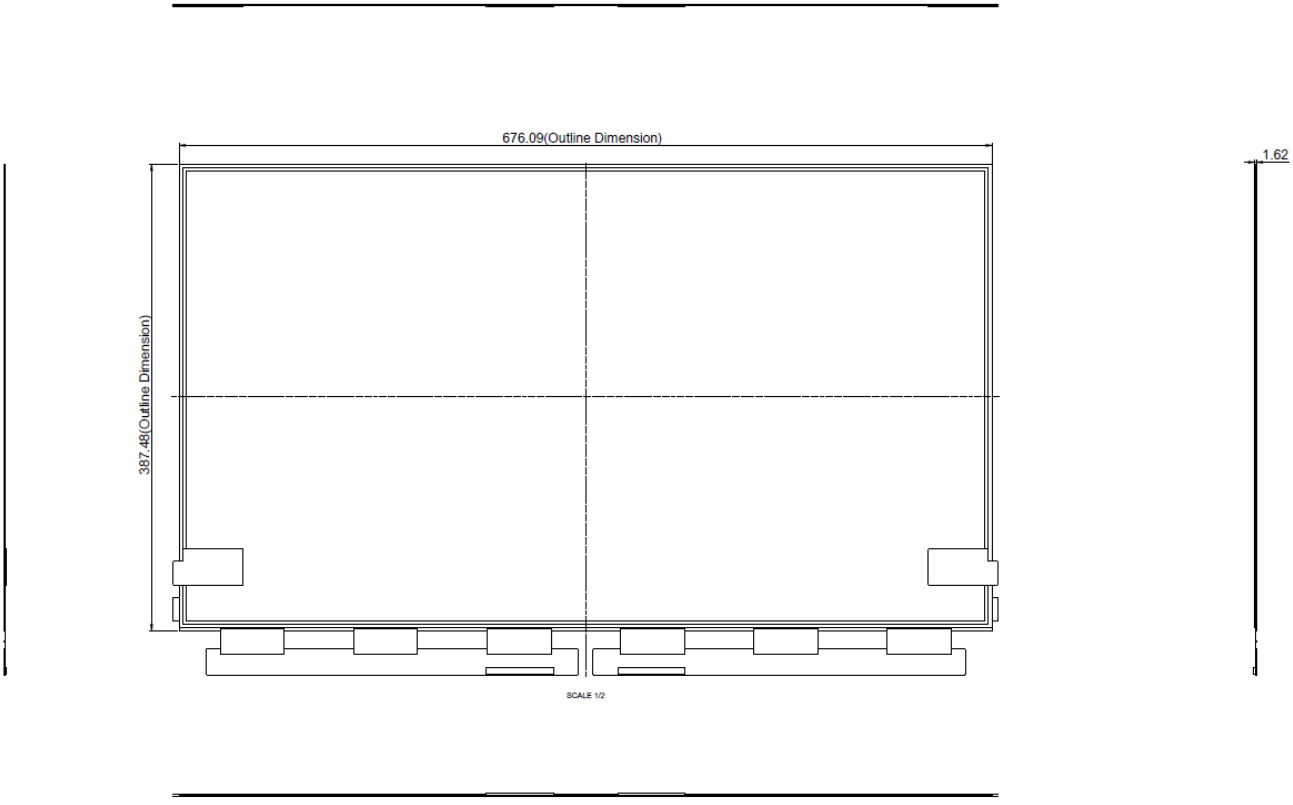
| Item | Value | |
|---|---|---|
| Outline Dimension (Sealing Board Ass'y) | Horizontal | 676.09mm(TBD) |
| | Vertical | 387.48mm(TBD) |
| | Thickness (at slimmest part) | 1.6mm(TBD) |
| Active Display Area | Horizontal | 664.29mm(TBD) |
| | Vertical | 373.48mm(TBD) |
| Weight | 1.04kg(W/O C-PCB) (TBD) | |

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

| Item | Value | |
|---|---|---|
| On Bezel (Active Area ~ Edge of Sealing Board ASS'y) | Horizontal | 5.9mm(Left) / 5.9mm(Right) (TBD) |
| | Vertical | 5.9mm(Top) / 8.1mm(Bottom) (TBD) |

**[Front View of Board Assem**

TBD

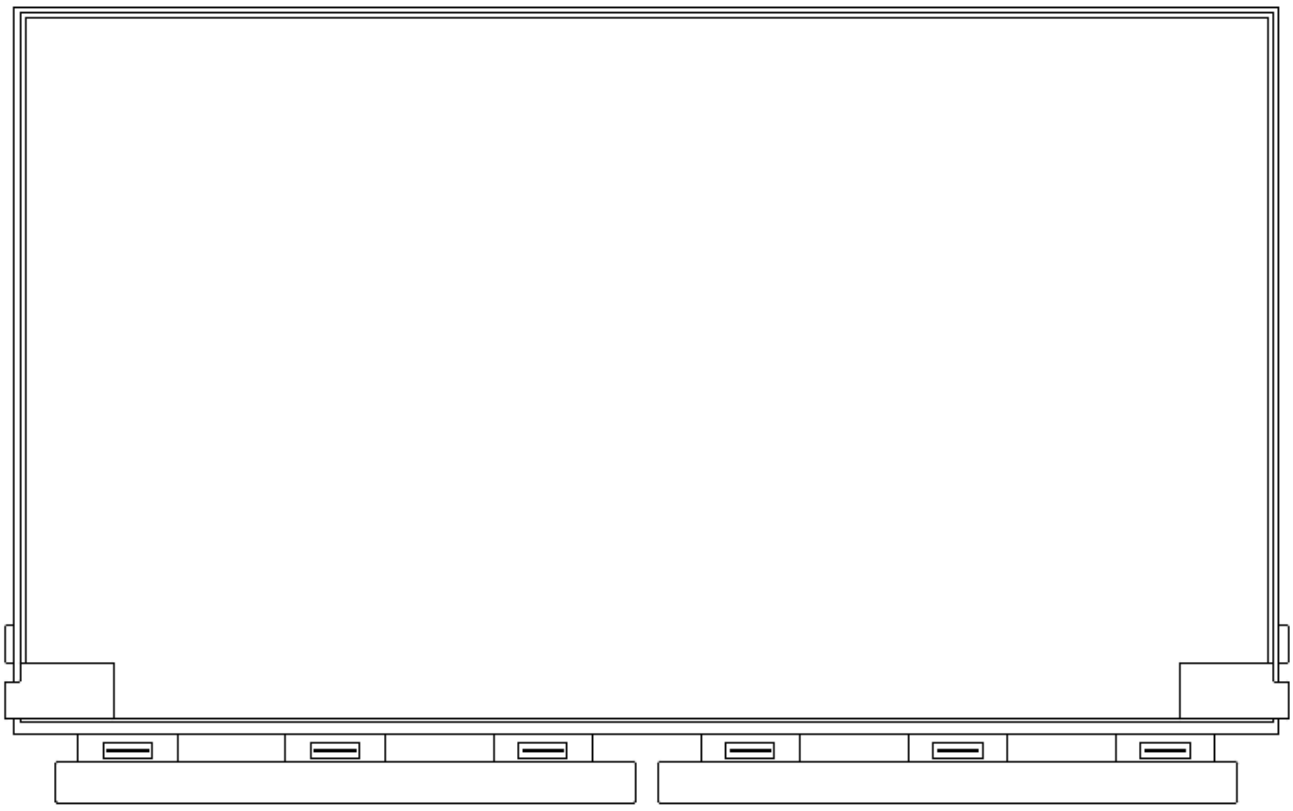



Note

1. Unspecified tolerance is ± 0.2mm

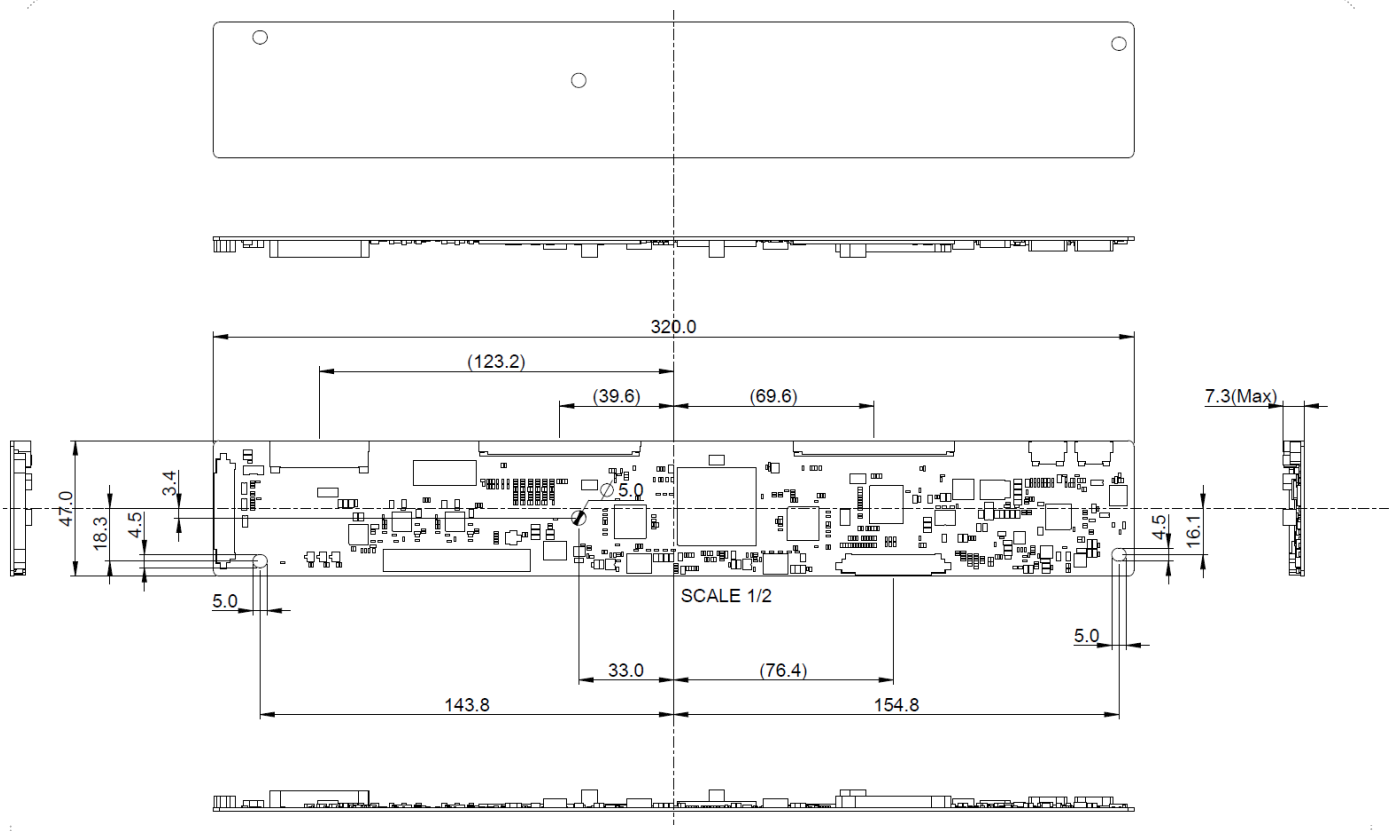
**[Rear View of Board Assem**

TBD



**[Control Board Assembly Dimension]**

TBD




**NOTE**

1. Unspecified tolerance is ±1.0mm

## 6. Reliability

**Table 17. ENVIRONMENT TEST CONDITION**

| No. | Test Item | Condition |
|---|---|---|
| 1 | High temperature storage test | Ta= 60°C 240h |
| 2 | Low temperature storage test | Ta= -20°C 240h |
| 3 | High temperature operation test | Ta= 50°C 50%RH 240h |
| 4 | Low temperature operation test | Ta= 0°C 240h |
| 5 | Pallet packing vibration test (non-operating) | Wave form : random<br>Vibration level : 2.0Grms<br>Bandwidth : 3-300Hz<br>Duration : Z, 60 min |
| 6 | Humidity condition Operation | Ta= 40 °C, 90%RH |
| 7 | Altitude operating<br>storage / shipment | 0 - 15,000 ft<br>0 - 40,000 ft |

Note : 1. Before and after Reliability test, OLED Module should be operated with normal function.

## 7. International Standa TBD

### 7-1. Safety

(1) IEC 62368-1, The International Electro-technical Commission(IEC).
Audio/video, Information and Communication Technology Equipment - Safety - Safety Requirements.

(2) EN 62368-1, European Committee for Electro-technical Standardization (CENELEC)
Audio/video, Information and Communication Technology Equipment - Safety Requirements

(3) UL 62368-1, UL LLC.
Audio/video, Information and Communication Technology Equipment - Safety Requirements.

(4) CAN/CSA C22.2 No.62368-1, Canadian Standards Association (CSA).
Audio/video, Information and Communication Technology Equipment - Safety Requirements

(5) IEC 60065, The International Electro-technical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements

### 7-2. Environment

(1) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council

# 8. Packing

## 8-1. Information of OLED Module Label

(1) Lot Mark

| A | B | C | D | E | F | G | H | I | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

| Year | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mark | K | L | M | N | P | Q | R | S | T | U | V |

2. MONTH

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Spe | Oct | Nov | Dec |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |

(2) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the OLED module.
This is subject to change without prior notice.

## 8-2. Packing Form

(1) Package quantity in one Pallet : 60 pcs
(10*pcs/Packing * 6packings = Total 60 pcs/pallet)

(2) Pallet Size : 1140 mm(W) X 910 mm(D) X 1140 mm(H)

## 9. Precautions

Please pay attention to the followings when you use this OLED Board Assembly.

### 9-1 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, Image Retention is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to Module. Otherwise, Module can't be operated its full characteristics perfectly.
(7) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal Module a fatal blow)
(8) Please do not set OLED on its edge.

### 9-2. Electrostatic Discharge Control

Since a Board Assembly is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

### 9-3. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

### 9-4. Storage Precautions

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they are stored in the container in which they were shipped.
(3) Wet bulb temperature should be Max 39°C, and no condensation of water.
(4) It must be stored in AL Bag packing

## 9-5. Handling Precautions

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) The Glass Encap surfaces(Rear of Board Assembly) should not be any residual moisture & Salinity.
- Always handle the Board Assembly with gloves.
- Chlorine or water from human sweat can accelerate the corrosion of Glass encapsulation
- Glass Encap surface should be protected by the moisture, salinity

(4) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.
Using a dry towel or fabric, remove water or solution like a cleaner from Board Assembly after finishing the install
- Do not use the cleaner containing acid or chlorine ingredient

(5) Be careful that the washing droplet is not flooded into the border gap on the panel edge, when cleaning the surface of OLED Module. It may cause abnormal operating or a malfunction in the OLED Module.

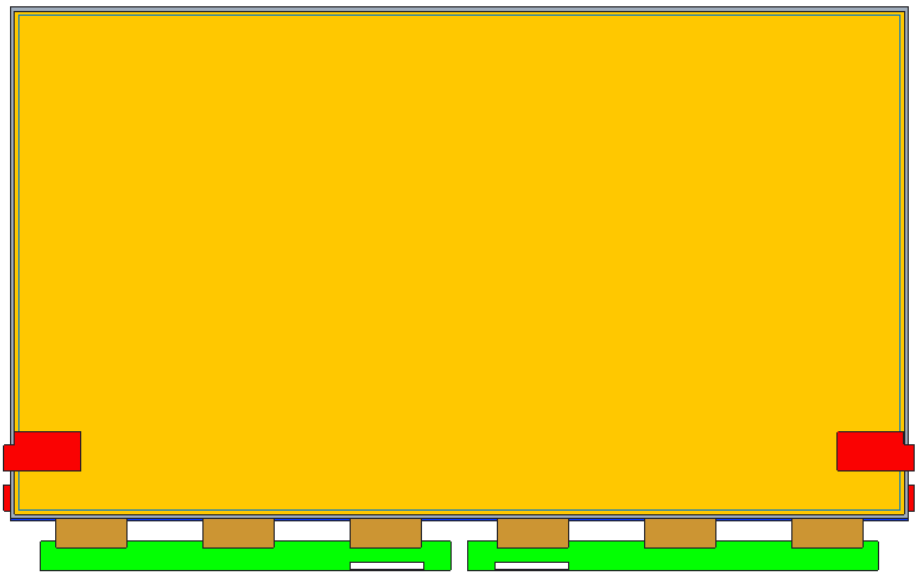
(6) When the OLED Module is assembled , mechanical stress may not be put on the panel.

(7) Be careful not to place any extra mechanical stress to the OLED module when designing the set .

(8) Be cautious not to any extra strong force (mechanical shock, strong tapping, shooting etc.) to the OLED module. It may cause abnormal operating or a malfunction in the OLED Module.

(9) If the panel is broken, glass should be kept away from the eyes and mouth. When it comes to contact to hands, legs, skin, or clothes, wash thoroughly with soap, and seek medical attention if necessary.

(10) Surface temperature of the Component on PCB should be controlled under 100℃ with TV Set status.
If not, problems such as IC damage or decrease of lifetime could occur.



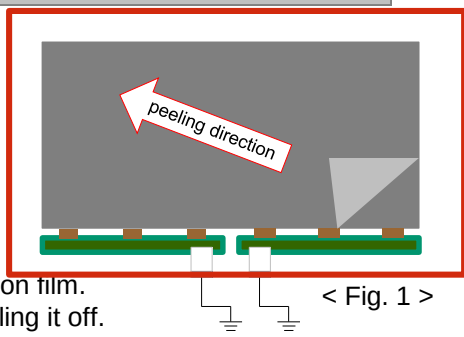
[Board Assembly ]

## 9-6. Appropriate Condition for Commercial Display

- To extend the lifetime and optimize a function of module, the below-mentioned operating conditions are required.

(1) Operating usages to reduce the risk of image sticking due to static image
a. OLED compensation should need.
- Refer to the 3-6-3. OLED compensation operation(Page19).
b. Information display recommended to use with moving picture.
c. Logo (image) and characteristics
- Logo image recommended not to use.
If needed, recommend that its position needs to be periodically shifted.
- Change colors themselves periodically.
d. The below-mentioned conditions are not recommended .
- Combination of Logo( or character) and background with largely different luminance.
- Using a single moving picture. (Recommend to use several different moving pictures.)
- The masked image with aspect ratio other than 16:9
- The division of screen
Note1) Abnormal condition just means conditions except normal condition.
Note2) Black image or moving image is strongly recommended as a screen saver.

(2) If the module will be used under severe conditions such as high temperature, high humidity, display patterns or operation time etc., it is strongly recommended to contact LG Display for the advice about usage and applications. Otherwise, its reliability and function may not be guaranteed.



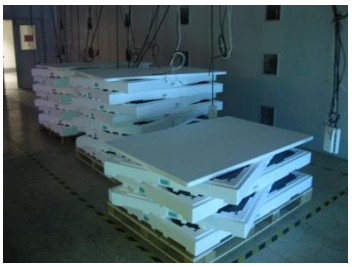

< Fig. 1 >

## 9-7. Protection Film

(1) Please don't remove the protection film before assembly.
(2) Please peel off the protection film slowly.
(3) Please peel off the protection film just like shown in the Fig.1
(4) Ionized air should be blown over during the peeling.
(5) Source PCB should be connected to the ground when peel off the protection film.
(6) The protection film should not be contacted to the source D-IC during peeling it off.
(7) When handling the H/C Film, in particular, please be aware of the following precautions.
- Please do not damage on the edge of the polarizer in any form.
- Peeling off the protection film must be done only with the adhesive tape, not with other means by fingers, tweezers and so on.
- It is recommended to peel off the protection film as slowly as possible at an initial step.
- Refer to Appendix – XIV for more details

## 9-8. B/A Box Pretreatment Precautions

In winter season , in particular, please be aware of the following precautions.
(1) Before putting B/A boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
(2) Place the lid open on the B/A box and allowed to stand for 24 hours in the similar environment of work place. It was shown in Fig.2



< Fig. 2>

TBD

## 9-9. Packing Precautions

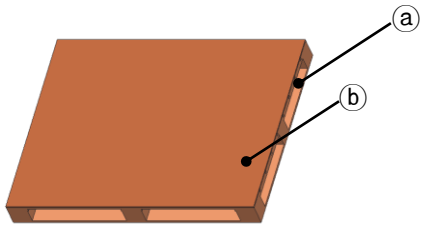
Product assembled into module should be stored in the Al-bag (cover case).

# # APPENDIX - I

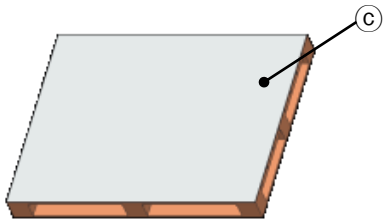
## ■ Pallet Ass'y

a) AL Sheet + B/Ass'y Qty + PE Sheet / Box : 1pcs + 10pcs + 11pcs
b) B/Ass'y Qty / Pallet : 60pcs
c) Oxygen Absorber + Desiccant / Box : 3ea + 5ea
d) Oxygen Absorber + Desiccant / Pallet : 18ea + 30ea
e) Box Qty / Pallet : 6Box

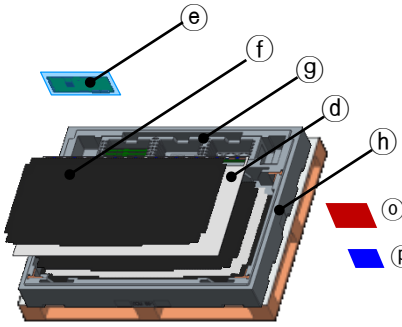
**1**




**2**



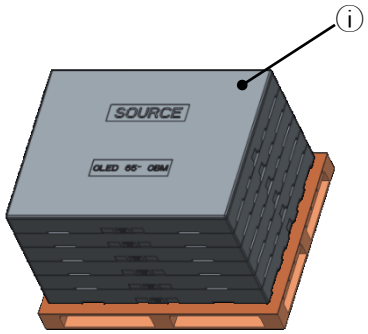

**3**



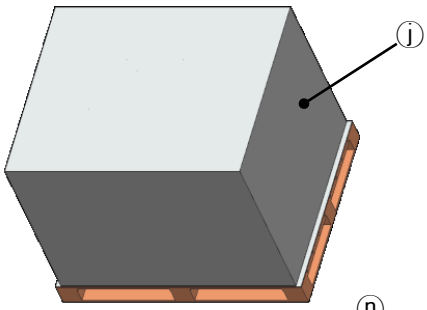

ⓞ Oxygen Absorber

ⓟ Desiccant

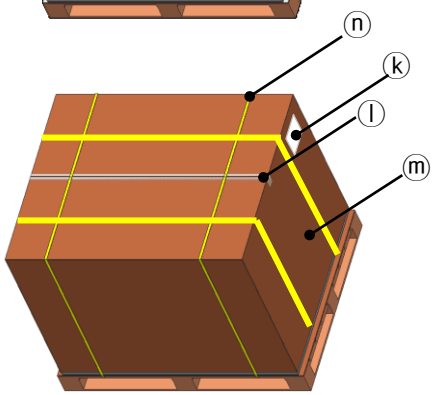
**4**




**5**



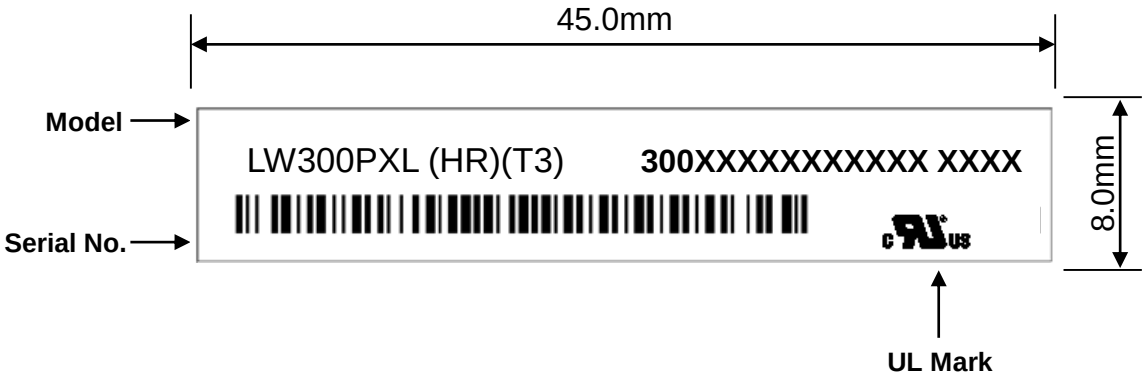

**6**



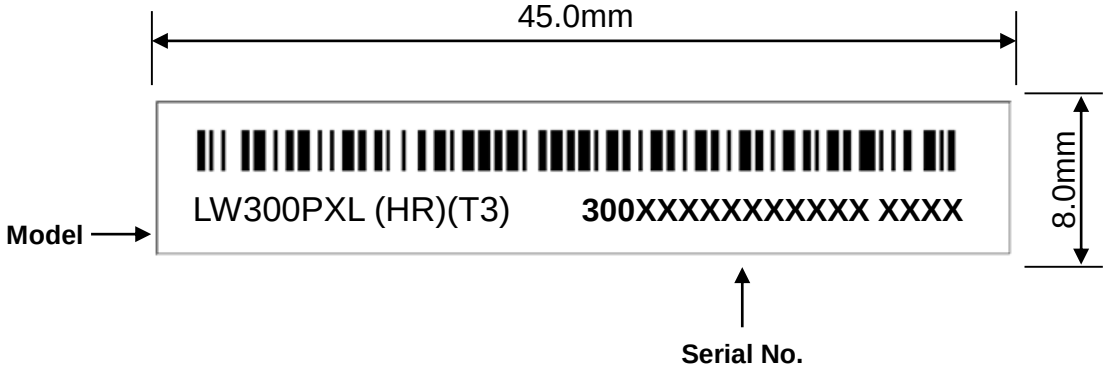

| No. | Description | Material |
|---|---|---|
| ⓐ | Pallet | Plywood |
| ⓑ | Carton Plate | Paper(SW) |
| ⓒ | AL Sheet | AL |
| ⓓ | Board Ass'y | - |
| ⓔ | Include TCON 1ea | - |
| ⓕ | PE Sheet | LDPE |
| ⓖ | C-PCB Packing | PP |
| ⓗ | Bottom Packing | EPS |
| | AL-Sheet | LDPE+AL |
| ⓘ | Top Packing | EPS |
| ⓙ | AL Bag | AL |
| ⓚ | Label | YOPO |
| ⓛ | Tape | OPP |
| ⓜ | Angle Packing | Paper(SW) |
| ⓝ | Band | PP |
| ⓞ | Oxygen Absorber | |
| ⓟ | Desiccant | |

# **APPENDIX - II**

■ Board Ass'y Label

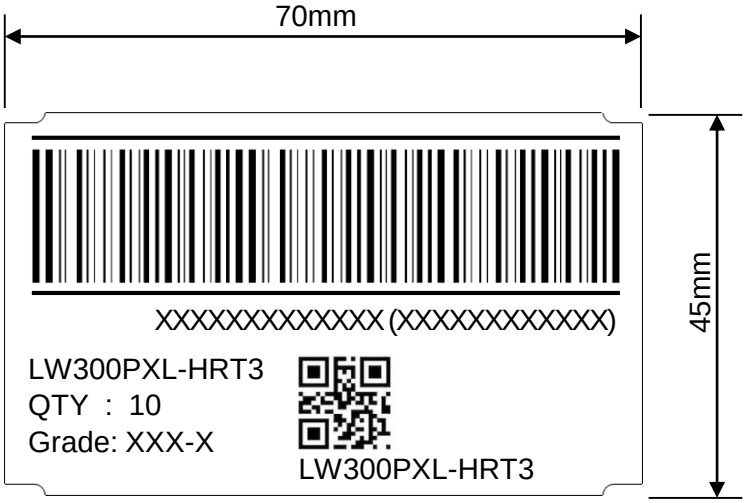



■ Control PCB Label

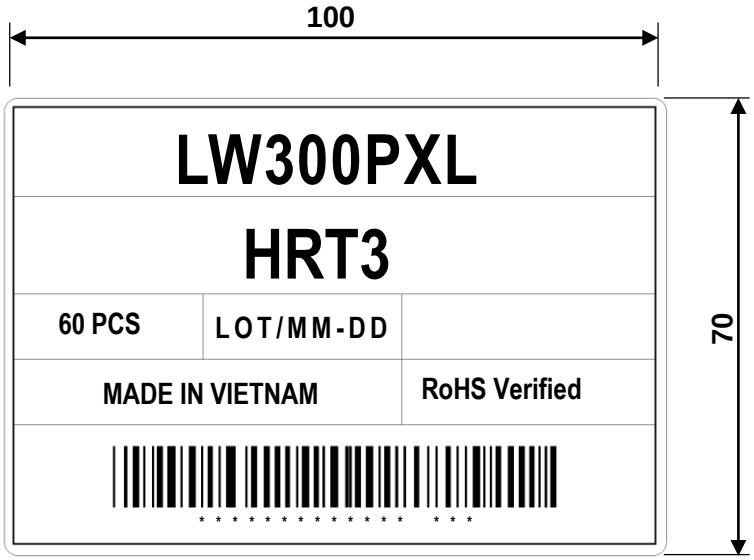


## # APPENDIX - III

### ■ Box Label



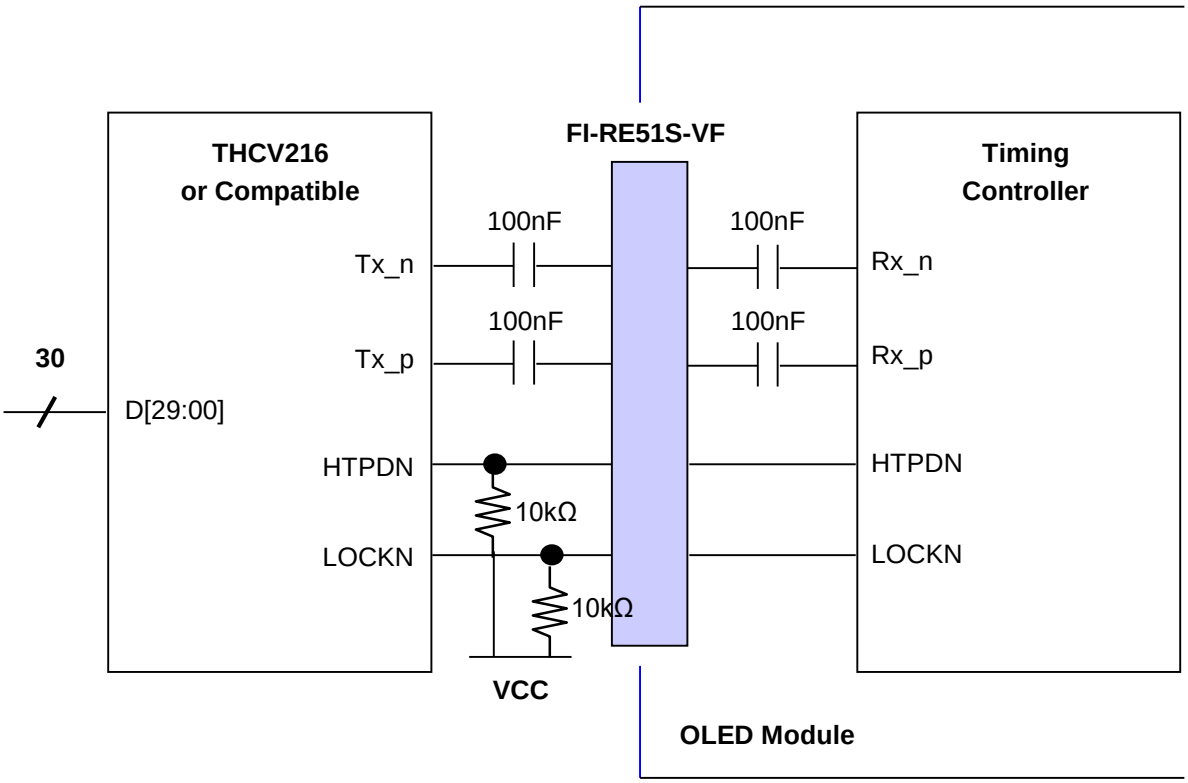

### ■ Pallet Label




* LGD Haiphong : MADE IN VIETNAM

## # APPENDIX - IV

■ Required signal assignment for Flat Link (Thine : THCV216) Transmitter



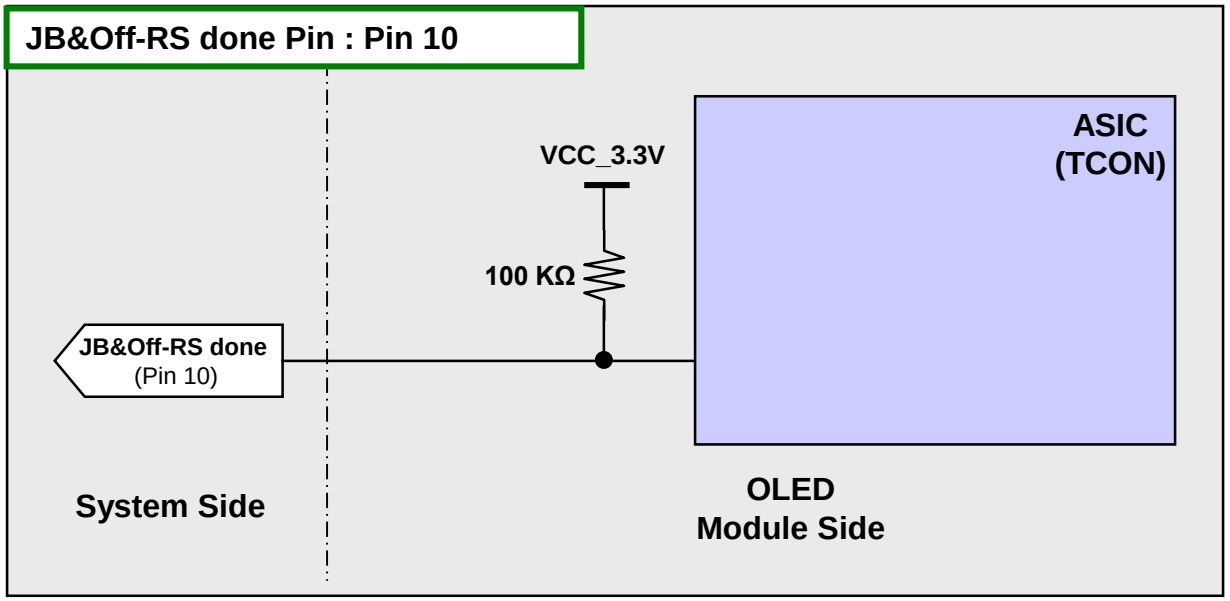

Note: 1. The OLED module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to VbyOne Transmitter Data Sheet for detail descriptions. (THCV216 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 9.

# APPENDIX - V-1

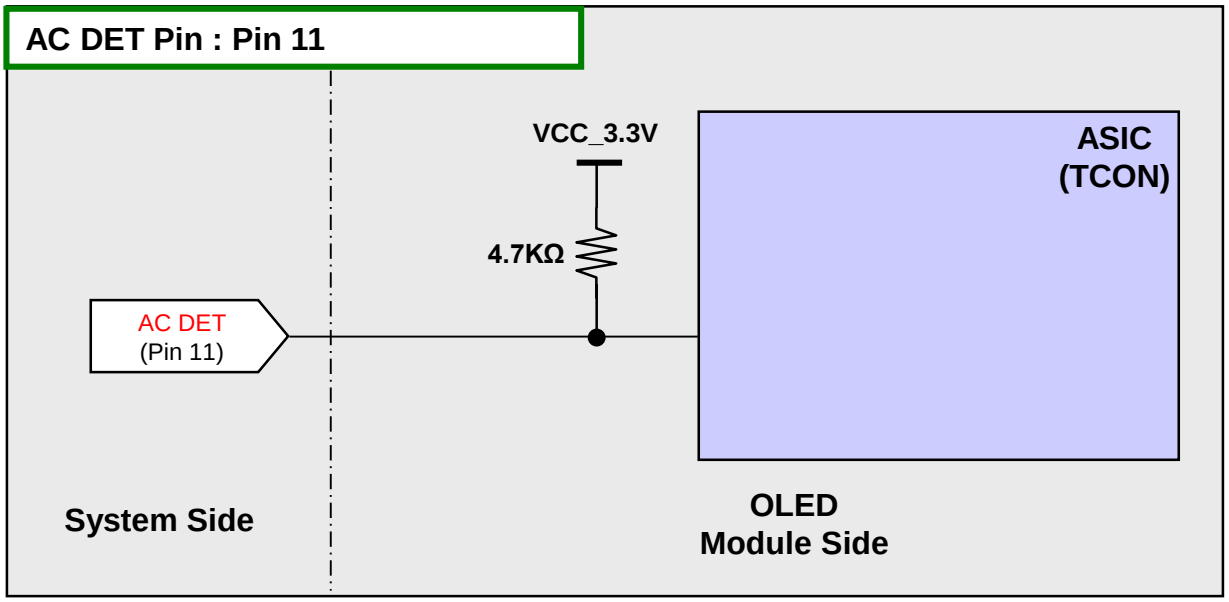
## ■ Circuit Block Diagram for Option Pin

TBD

(1) Circuit Block Diagram of **JB&Off-RS done** pin




(2) Circuit Block Diagram of AC_DET pin

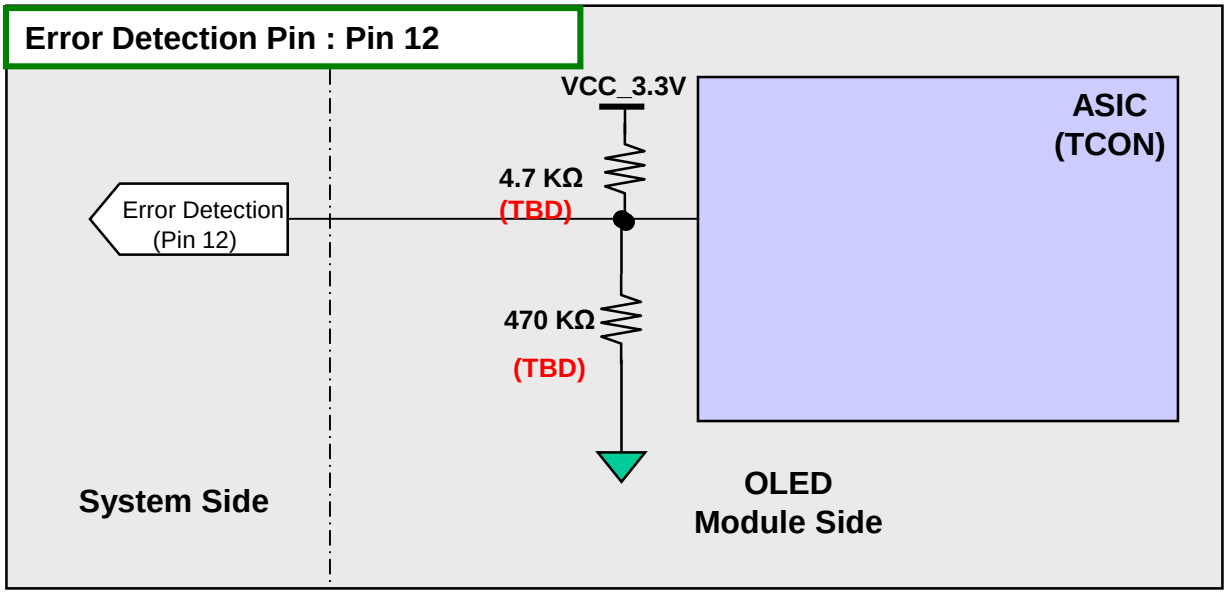


# APPENDIX - V-2

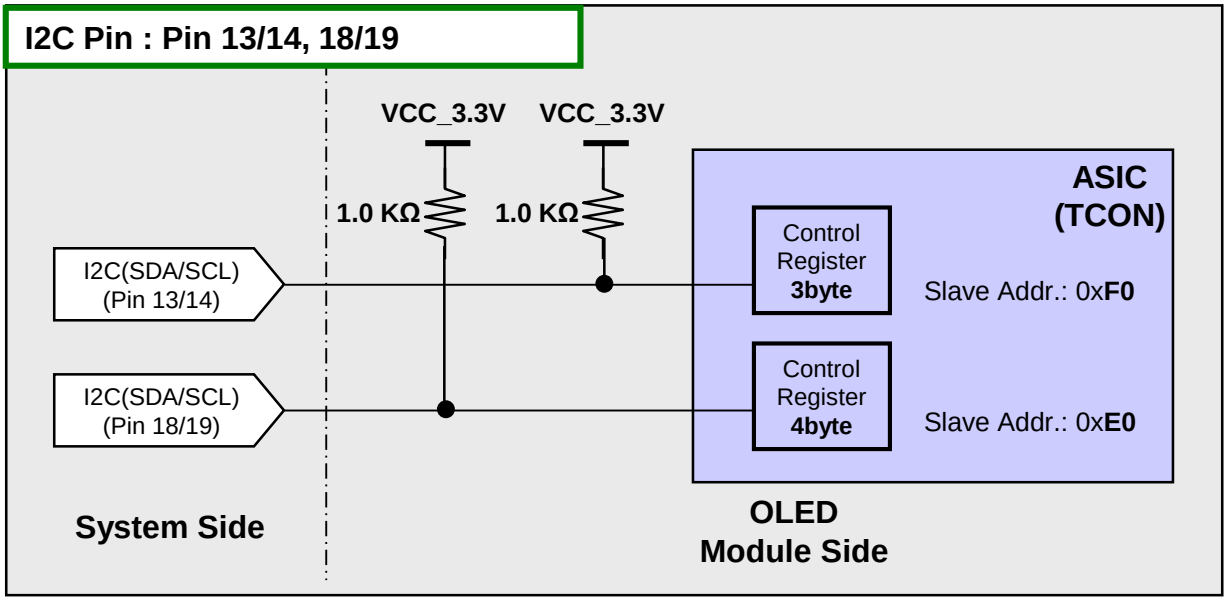
## ■ Circuit Block Diagram for Option Pin

TBD

(3) Circuit Block Diagram of **Error Detection** pin




(4) Circuit Block Diagram of **I2C(SDA/SCL)** pin

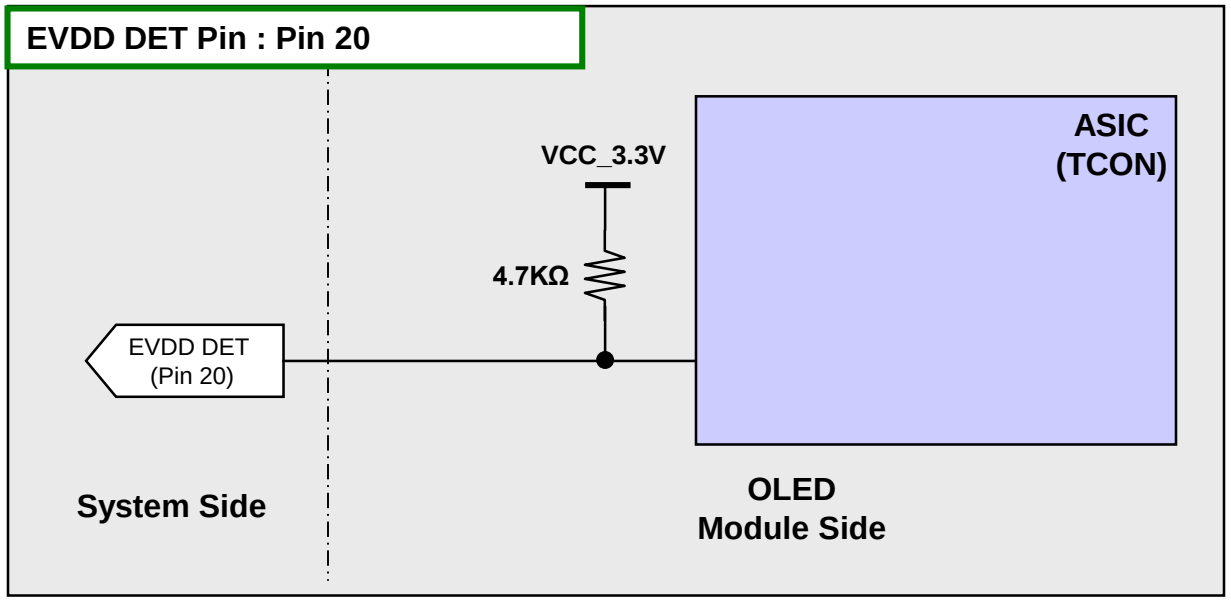


# APPENDIX - V-3

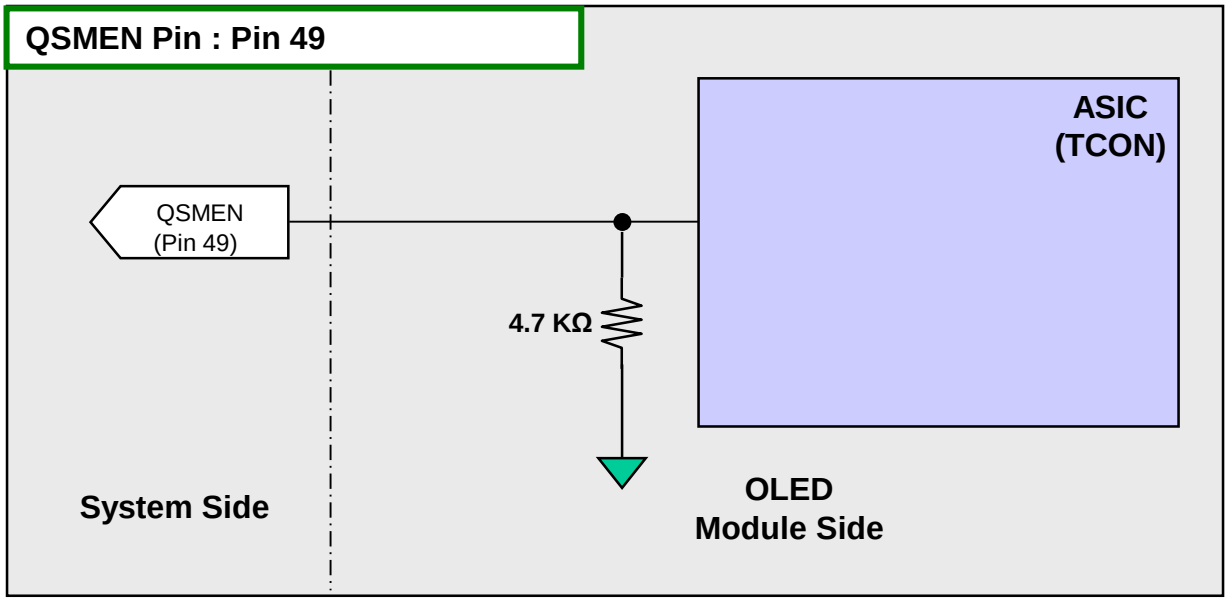
## ■ Circuit Block Diagram for Option Pin

TBD

(5) Circuit Block Diagram of EVDD DET pin




(6) Circuit Block Diagram of **QSMEN** pin

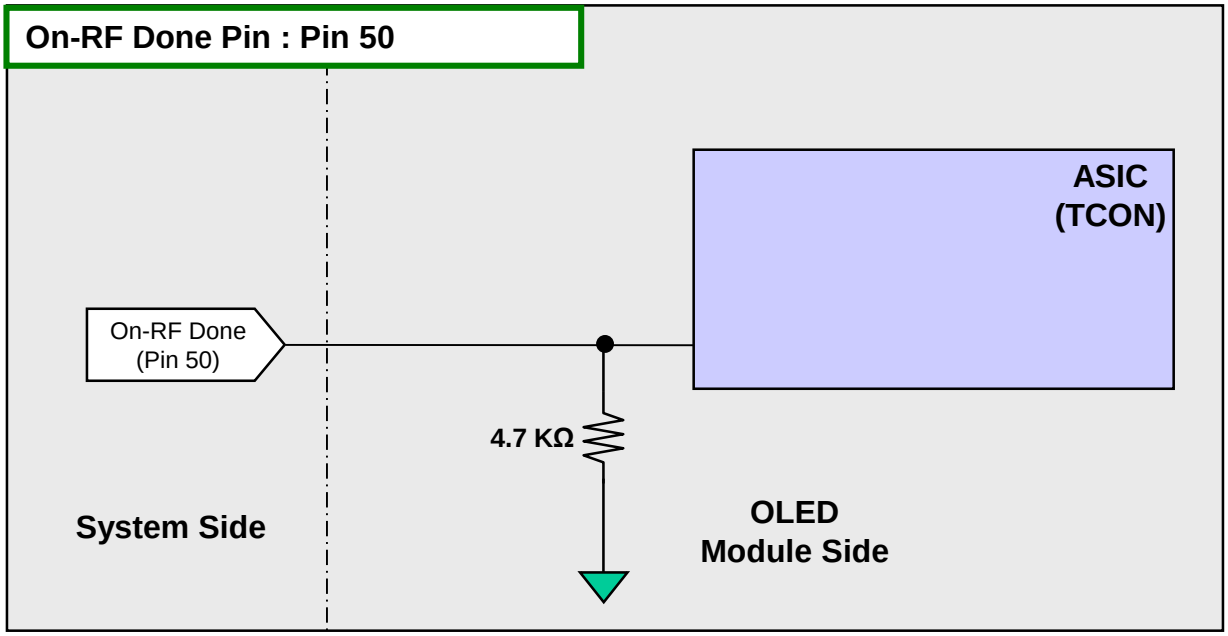


# APPENDIX - V-4

## ■ Circuit Block Diagram for Option Pin

TBD

(7) Circuit Block Diagram of **On-RF Done** pin



# APPENDIX- VI

TBD

## ■ ASIC Firmware

| Category | FW version Value | Checksum Value |
|---|---|---|
| Pre-CAS | TBD | TBD |

## ■ Register map

The following register is controlled by I2C Interface.

| | Bit[7]: MSB | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0]: LSB |
|---|---|---|---|---|---|---|---|---|
| **Addr : 0x001** | **CPC EN** | **TPC EN** | **Not Use** | **OFF RS EN** | **Not Use** | **Not Use** | **Not Use** | **Not Use** |

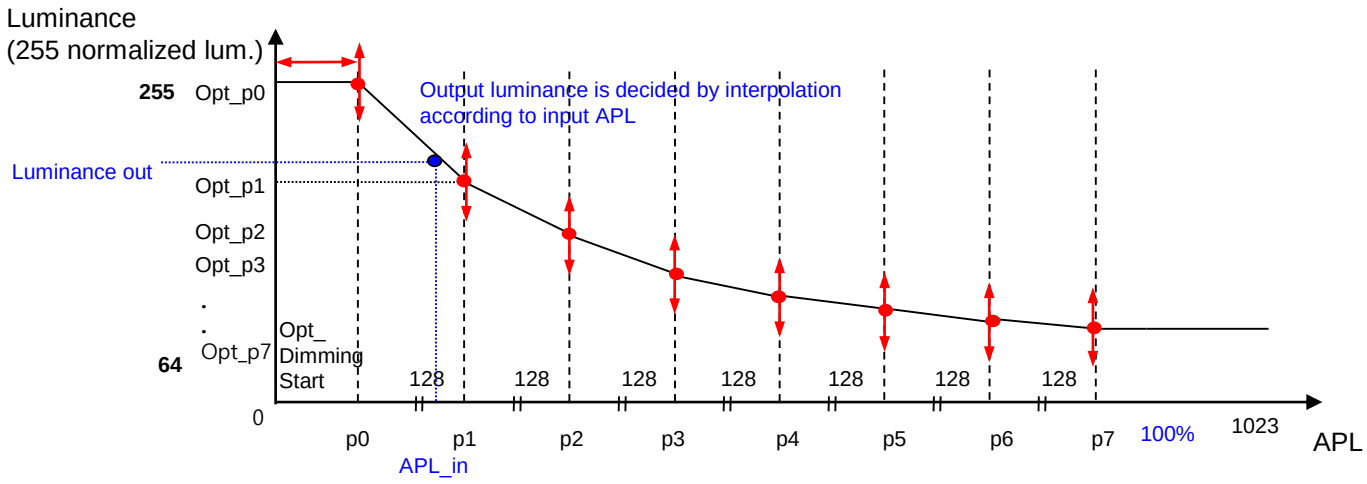
**Device Address: 0xE0**

| Address [HEX] | Register Name | Description | Remark |
|---|---|---|---|
| 0x000 | Valid | Read only register (LGD use) | |
| 0x001 | [7] : CPC enable | 1: enable (default), 0: disable | |
| | [6] : TPC enable | 1: enable (default), 0: disable | |
| | [5] : Not use | LGD reserved | |
| | [4] : Off RS enable | 1: enable, 0: disable | |
| | [3] : Not use | LGD reserved | |
| | [2] : Not use | LGD reserved | |
| | [1:0] : Not use | LGD reserved | |
| 0x002 | Not use | | |
| 0x003 | Opt_p0 | APL P0 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x004 | Opt_p1 | APL P1 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x005 | Opt_p2 | APL P2 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x006 | Opt_p3 | APL P3 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x007 | Opt_p4 | APL P4 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x008 | Opt_p5 | APL P5 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x009 | Opt_p6 | APL P6 point corresponds to the 255 normalized luminance | Value Range: 0~255 |
| 0x00A | Opt_p7 | APL P7 point corresponds to the 255 normalized luminance | Value Range: 0~255 |

TBD

| Address [10:0] | Register Name | Description | Remark |
|---|---|---|---|
| 0x00B | [7] : Not used | LGD reserved | |
| | [6:5] : LEA mode sel [1:0] | b00: Normal operation, **b01 / b10 / b11: LGD reserved** | |
| | [4] : LEA refresh mode en | 1: LEA Refresh, 0: Normal LEA | |
| | [3] : HDR_en | 1: Enable, 0: Disable | |
| | [2]: Not use | LGD reserved | |
| | [1:0] : Not use | LGD reserved | |

## ❑ PLC curve parameter



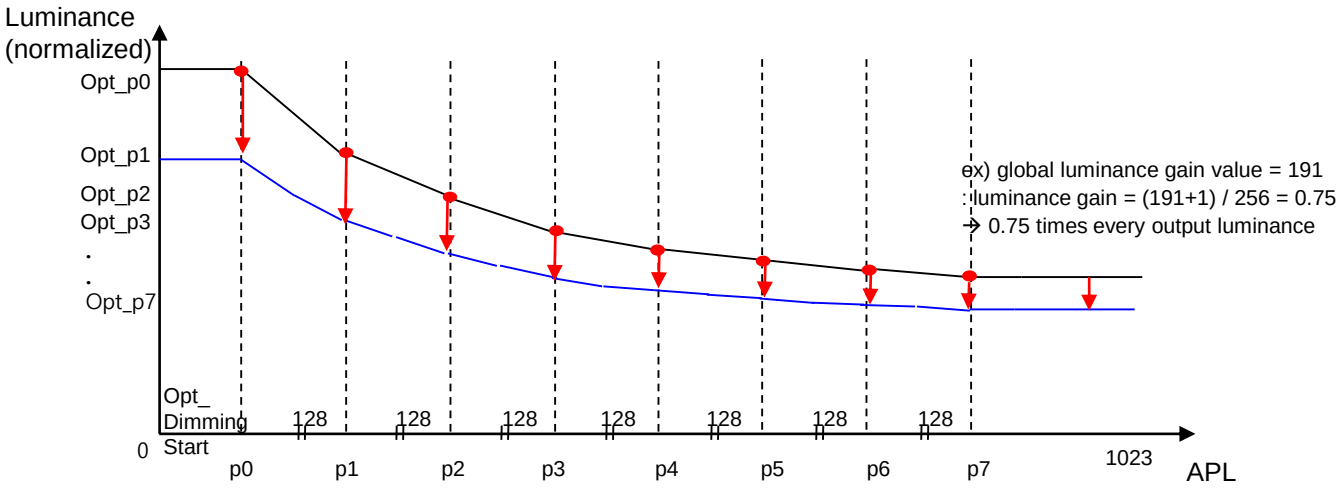

Every interval between each points except P0 is fixed to 128

- Luminance of p7~1023 interval are Opt_p7
- The point over 1023 is discarded

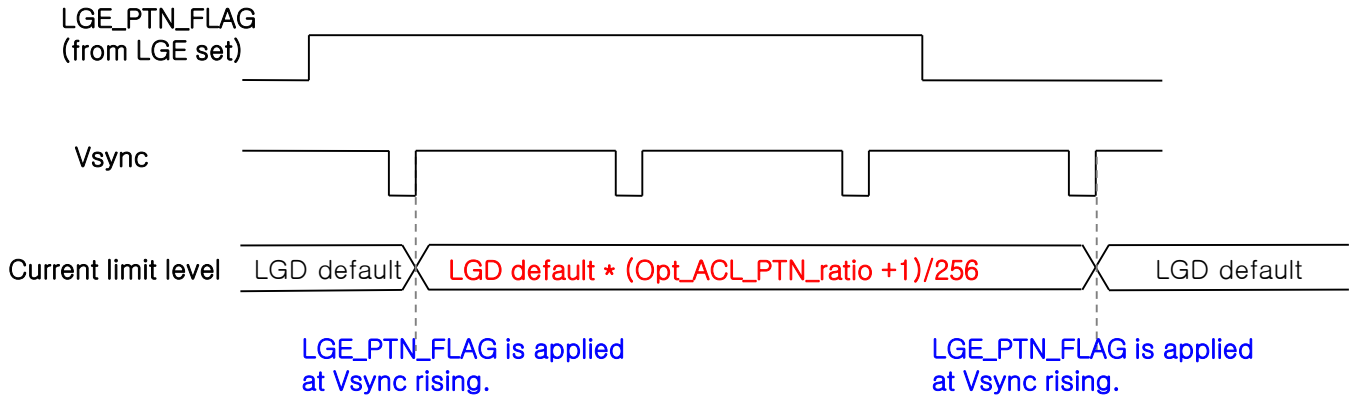
TBD

| Address [Hex] | Register Name | Description | Remark |
|---|---|---|---|
| 0x016 | Opt_global_luminance_gain | Adjust global luminance gain<br>0~1 luminance gain according to 0~255 value<br>(Same luminance gain is applied to every P0~P7 points) | Value Range: 0~255 |
| 0x017 | Opt_ACL_PTN_ratio | Adjust ACL level gain for LGE PTN detect | Value Range: 0~255 |
| 0x054 | [7] Power Off Enable | 1: Enable, 0: Disable (JB Update) | |
| | [6:0] Not used | LGD reserved | |
| 0x05D | [7] JB Enable | 1: Enable, 0: Disable(JB Operation) | |
| | [6:0] Not used | LGD reserved | |
| 0x05E | Test_temp[15:8] | temperature sensor | Read only |
| 0x05F | Test_temp[7:0] | | |

## ❑ Global luminance gain




## ❑ Current limit level changes according to LGE PTN detect



**# APPENDIX- VII-1** TBD

# Gray to Gray Response Time Uniformity

This is only the reference data of G to G and uniformity for for LW330PXL-HRT3 model.

1. G to G Response Time :
   Response time is defined as FIG.1. and shall be measured by switching the input signal for "Gray (N) " and "Gray(M)".(32Gray Step at 8bit)

2. G to G Uniformity
   The variation of G to G Uniformity , $\delta_{G\ to\ G}$ is defined as :

$$\text{G to G Uniformity} = \frac{Maximum(GtoG) - Typical(GtoG)}{Typical(GtoG)} \leq 1$$

*Maximum (GtoG) means maximum value of measured time (N, M = 0 (Black) ~ 1023(White), 128 gray step).

| | 0Gray | 127ray | 255Gray | … | 895Gray | 1023Gray |
|---|---|---|---|---|---|---|
| 0Gray | | TrR:0G→127G | TrR:0G→255G | ... | TrR:0G→895G | TrR:0G→1023G |
| 127Gray | TrD:127G→0G | | TrR:127G→255G | ... | TrR:127G→895G | TrR:127G→1023G |
| 255Gray | TrD:255G→0G | TrD:255G→127G | | ... | TrR:255G→895G | TrR:255G→1023G |
| … | ... | ... | ... | | ... | ... |
| 895Gray | TrD:895G→0G | TrD:895G→127G | TrD:895G→255G | ... | | TrR:895G→1023G |
| 1023Gray | TrD:1023G→0G | TrD:1023G→127G | TrD:1023G→255G | ... | TrD:1023G→895G | |

3. Sampling Size : 2 pcs

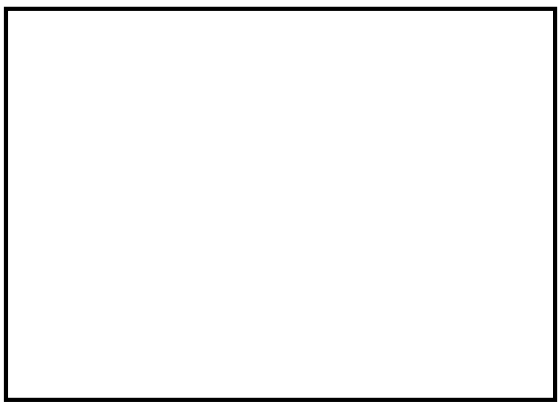
4. Measurement Method : Follow the same rule as optical characteristics measurement.

5. Current Status

   Below table is actual data of production on **XX. XX. XXXX (LGD DV Event Sample)**

| | G to G Response Time [ms] | | Average |
|---|---|---|---|
| | Min. | Max. | |
| # 1 | | | |

**FIG. 1**



< # 1 >

# APPENDIX- VII-2

TBD

## ■ MPRT Response Time Uniformity ($\delta_{MPRT}$)

This is only the reference data of MPRT and uniformity for for LW330PXL-HRT3 model.

(1). MPRT Response Time :
Response time is defined as FIG. 4.

(2). MPRT Uniformity
The variation of MPRT Uniformity , $\delta_{MPRT}$ is defined as :

$$\text{MPRT Uniformity} = \frac{Maximum\ (MPRT) - Typical\ (MPRT)}{Typical\ (MPRT)} \leq 1$$

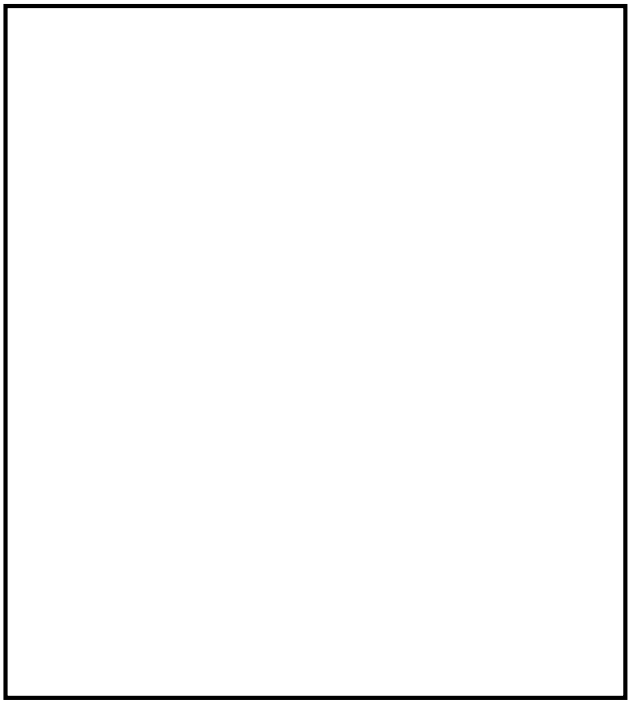
(3). Sampling Size : 1 pcs

(4). Measurement Method : Follow the same rule as optical characteristics measurement.

(5). Current Status

Below table is actual data of production on **XX. XX. XXXX (LGD DV Event Sample)**

| Sample | MPRT Response Time [ms] | | Average |
|---|---|---|---|
| | Min. | Max. | |
| # 1 | | | |



# APPENDIX –VIII

## ■ PLC Curve

(1) It is recommended to the set the TV Set Peak Luminance to 50% of the Module Peak Luminance at P0 point in Default display mode for considering power savings and prevention of Image retention.
(Fig. 1. Set PLC Curve )

- If End users watch videos with fixed images such as broadcast logos for a long time at the level of Module Peak luminance, there is a risk of image retention defects.
Therefore, the shipping mode luminance control can proactively prevent the risk of image retention defects.
- If customer need to promote the Picture Quality, It is recommended to user store mode.
- It is recommended that the HDR function be applied to the module shipment condition, 'HDR Off'.

(2) It is recommended to automatically operate the light sensor 'On' in Set shipping mode.
- It is recommended to prevent the risk of eye fatigue and image retention defects through the user of appropriate illumination depending on the user's environment.

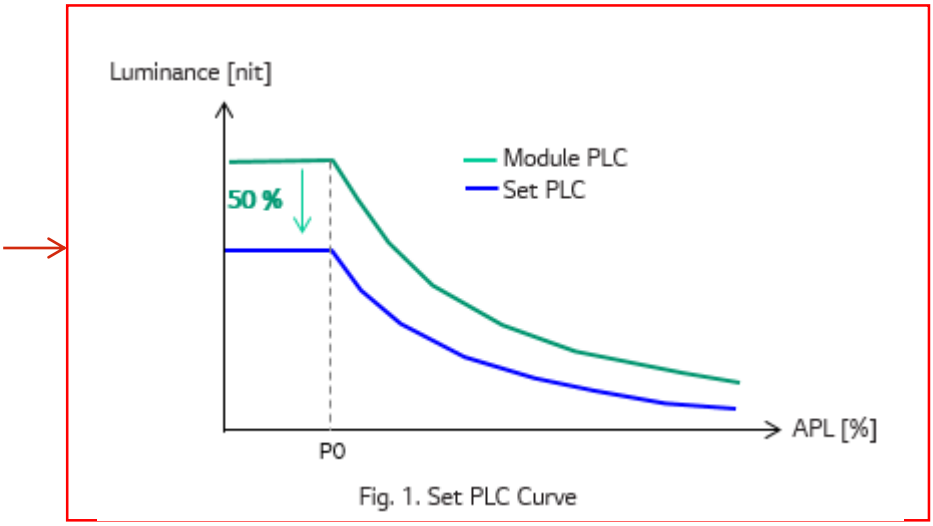


Fig. 1. Set PLC Curve

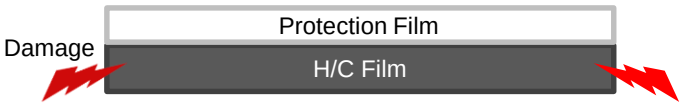
※ Default Display mode(End-user) : Set Peak Luminance ≤ 50% of Module Peak Luminance
※ Shipment mode : Picture mode first used by end-users after factory shipments
ex) Standard mode

## # APPENDIX- IX

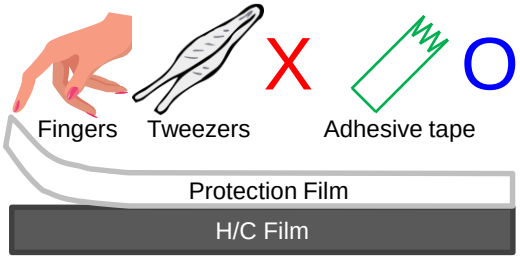
### ■ Things to avoid to prevent the H/C Film from breakage

Any kind of damage on the edge of the polarizer is not allowed. <Fig.1>

Use an adhesive tape to peel off the protection film from the polarizer. <Fig.2>




<Fig.1>

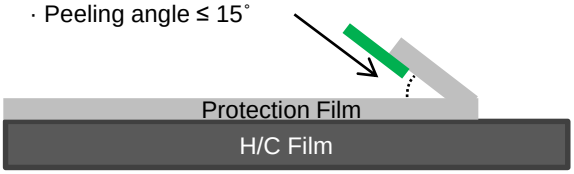



<Fig.2>

### ■ Recommended values for peeling velocity and angle

The values for peeling velocity and angle should be under 2m/min and 15 degrees each. <Fig.3>


· Peeling velocity ≤ 2m/min
· Peeling angle ≤ 15˚

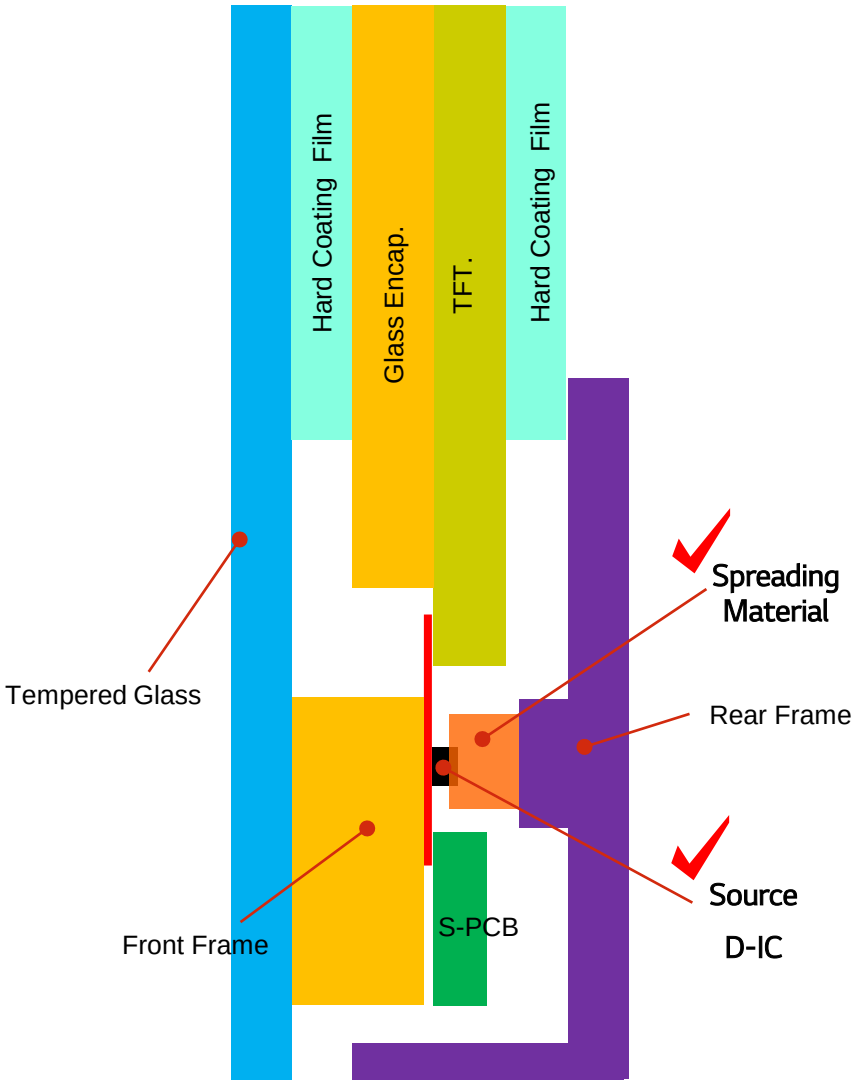



<Fig.3>

## # APPENDIX- X

## ■ Design guide for Heat dissipation for SOURCE D-IC

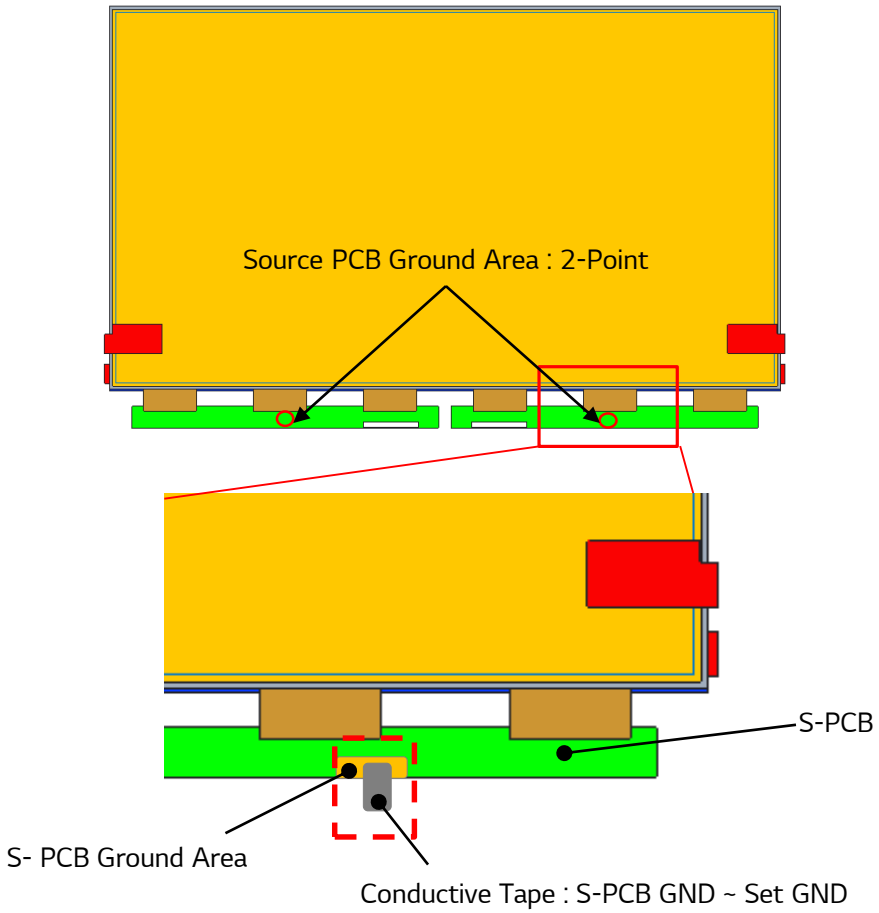
1. Potential issue
   The heat transfer efficiency down if D-IC is not contacted.
2. Recommendation
   In case of using Heat spreading sheet
   1) Contact the SOURCE D-IC with embossment on Heat spreading sheet for heat dissipation.
   2) Not be overlapped much to prevent COF damage.
   3) The contact area to exceed the area of the SOURCE D-IC.



## # APPENDIX- XI

## ■ Design guide for Electrostatic Discharging design for Board Assembly

1. Purpose
   To design the contact structure for electrostatic discharging on Board Assembly
2. Recommendation
   Electrostatic discharging design for Board Assembly (Ground Path)
   1) To design the contact structure for electrostatic discharging on Board Assembly
   2) Attach Conductive Tape or Equivalent between S-PCB Ground and Set Ground

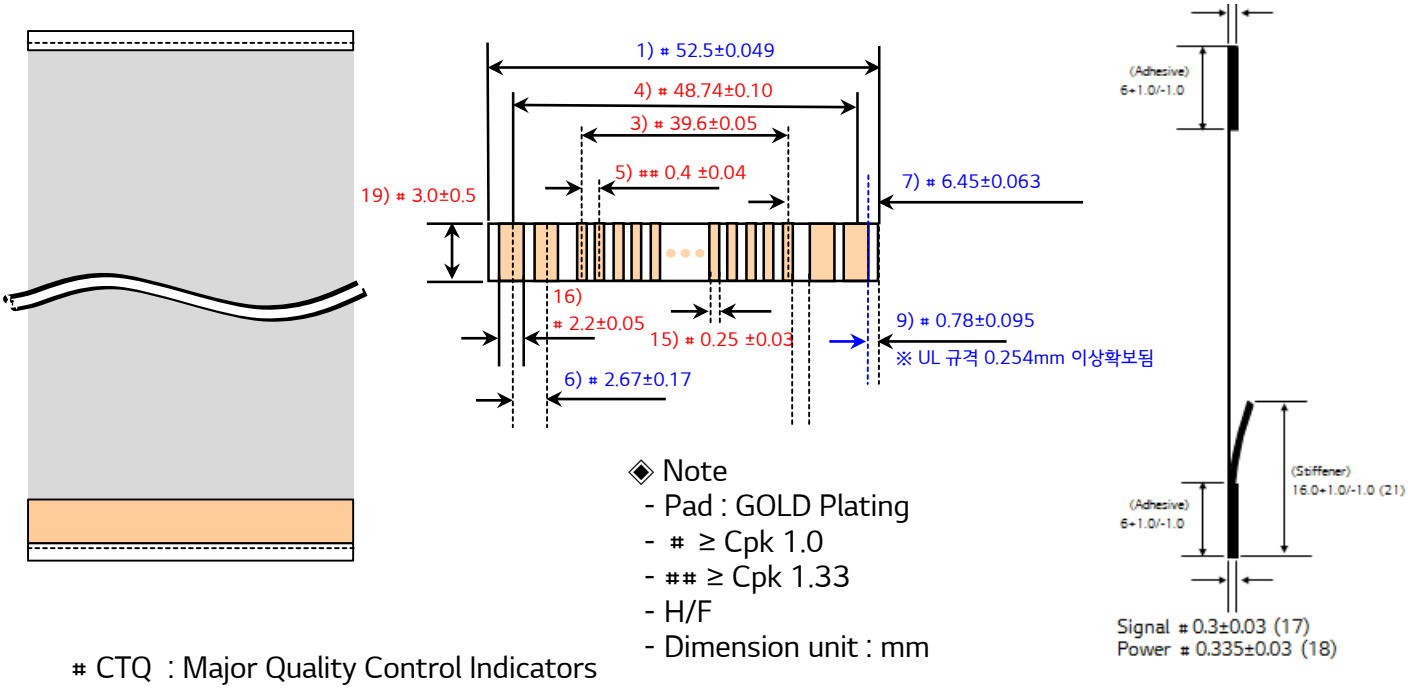


# APPENDIX - XII

## ■ FFC INFORMATION (OLED Connector)

- **S-PCB : TF43SW-100S/4-0.4SH** (manufactured by HIROSE)
- **C-PCB : TF43SW-100S/4-0.4SH (**manufactured by HIROSE)

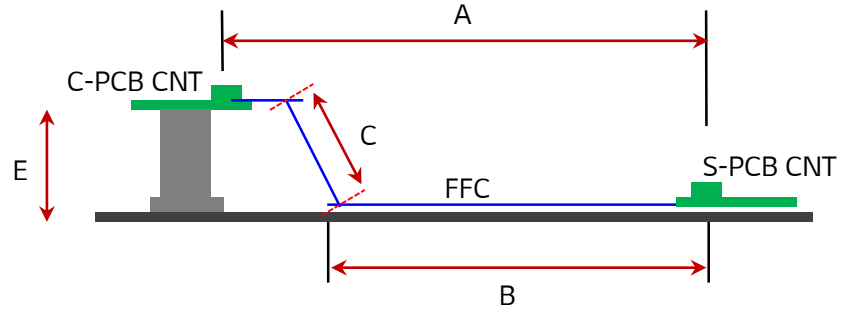
## ■ Drawing

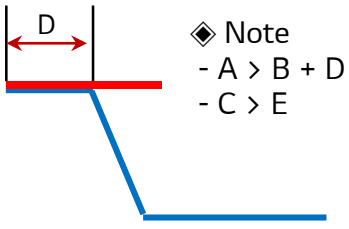



◈ Note
- Pad : GOLD Plating
- # ≥ Cpk 1.0
- ## ≥ Cpk 1.33
- H/F
- Dimension unit : mm

# CTQ : Major Quality Control Indicators
# Power Line : 2oz
# Signal Line : 2oz
# Impedance : 100 ohm (IMS Shield is Recommended)

## ■ Z-Bending guide



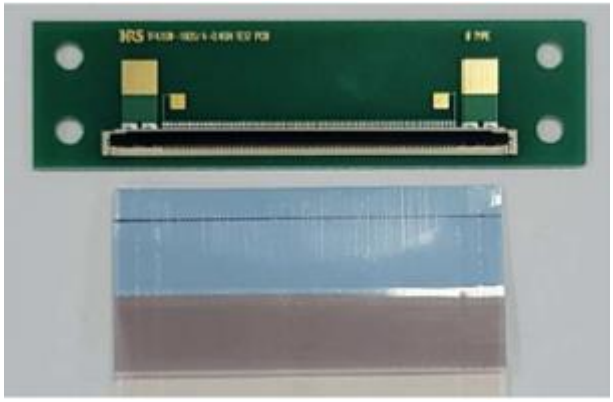

◈ Note
- A > B + D
- C > E

# The FFC must be folded in a Z-shape to prevent the FFC connector FLIP from being pressed or opened.
# In particular, it is necessary to use a gently folded Z-shape FFC for the slim set concept.

## # APPENDIX- XIII

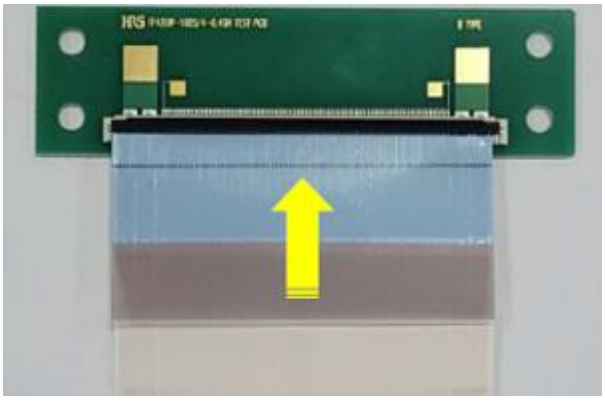
## ■ Guide for the FFC Connector fastening

### 1. Preparation for insert



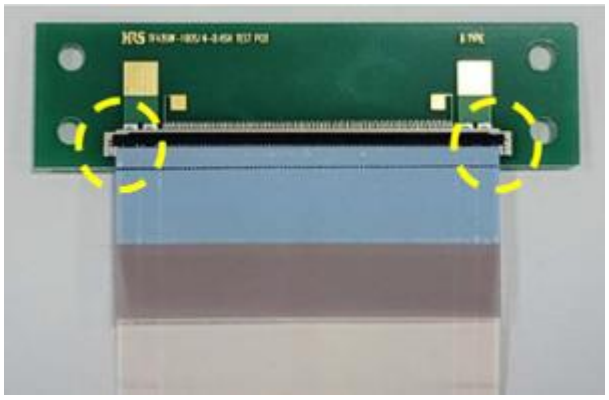
Place the FFC conductor face down and parallel to the connector.

### 2. Insertion



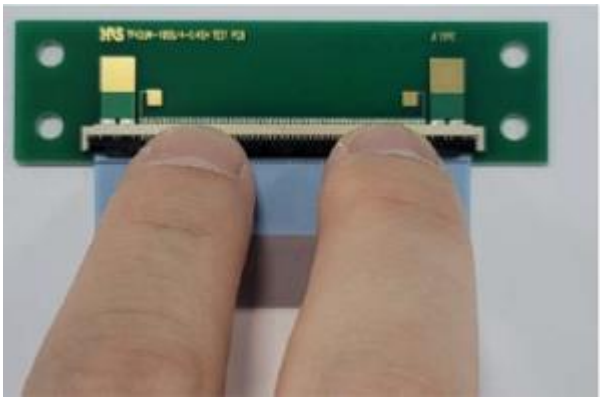
Insert the FFC horizontally and correctly without twisting.
When inserting from the corner as if swinging, it can be deformed by giving damage to the connector.

### 3. Completion of insertion



After the insertion, check the left and right sides Whether there is any abnormality.
(Non-inserted, twisted, inserted position)

### 4. Fastening



Fasten the actuator by closing the central part as if rotating.
(Because the connector is long, please close it using two fingers.)